X-ray Nanotomography Imaging for Circuit Integrity

The need for reliable and secure technological devices requires integrated circuits (ICs) that maintain integrity of the original design[1]. In order to keep costs low, ICs are often manufactured overseas[2]. Chip modifications, also called "Hardware Trojans" can be inserted in various phases of production, testing, and distribution, and be triggered later by pre-programmed timed or physical events, which can cause failure or compromise at key times during operation[3]. This can affect applications in fields as diverse as defense, aeronautic industry, consumer medical and financial records, and transportation security, for example. The authentication of IC chips to scan for Trojans can be complex because the type of modification can vary significantly, and is usually unknown in advance. Hence a thorough yet non destructive method for ensuring circuit integrity is required.

Photo: Krunkeworke/Flickr

Using the transmission x-ray microscope on Beam Line 6-2 at the Stanford Synchrotron Radiation Lightsource, based on an Xradia lab model[4], researchers from the University of Southern California Information Sciences Institute and Xradia Inc. have developed nanoscale computerized tomography (CT) methods to obtain nondestructive high resolution (30 nm) 3D images of integrated circuits that could be used to scan for defects and modifications. Because the ICs are very large compared with the microscope field of view (30 microns), complex methods for imaging the circuits and reconstruction of the 3D data were developed (Figure 1).

Because a 2D transmission image will reveal all absorbing objects penetrated by the x-ray path, tomography is necessary to combine views from different angles and reveal the different layers in the IC chip. A quick and robust method is required for scanning of chips, because of the large amounts of images required to cover a full chip area. Image registration algorithms are used to align multiple raster-scanned images at each angle, and then to align the tomographic data set with multiple angles. After image acquisition and reconstruction to form a 3D volume, individual layers of the chip could be distinguished with

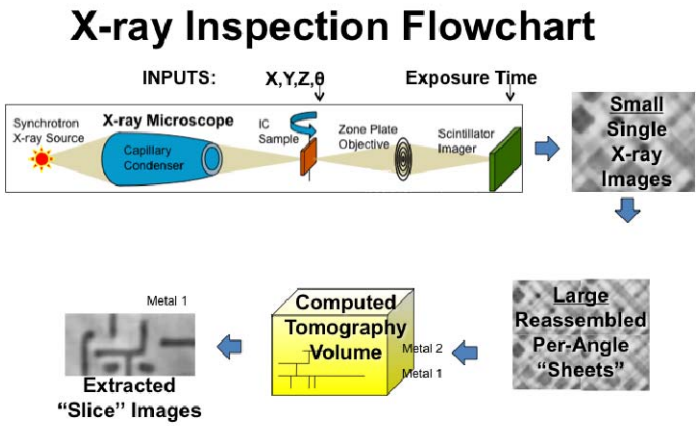

Figure 1. X-ray Inspection Flowchart: The chip sample is mounted on a motorized stage, and a control computer moves the stage to the required (x,y,z,θ) positions, sets the exposure times, and saves images from the CCD camera to disk. Raster-scanned images are reassembled for each angle and reconstructed to create a CT volume. Extracted slices from the CT volume reveal individual layers of the chip. (Figure adapted from Bajura et al. 2011)

the aid of a 3D visualization program. Slice imaging detail, which could be viewed and inspected for changes from the original design, is shown below in Figure 2 and in the movie. The synchrotron x-ray energy can also be tuned to image above and below the x-ray absorption edge of specific metals within the chips to view gate and active areas, and back end wiring interconnect layers.

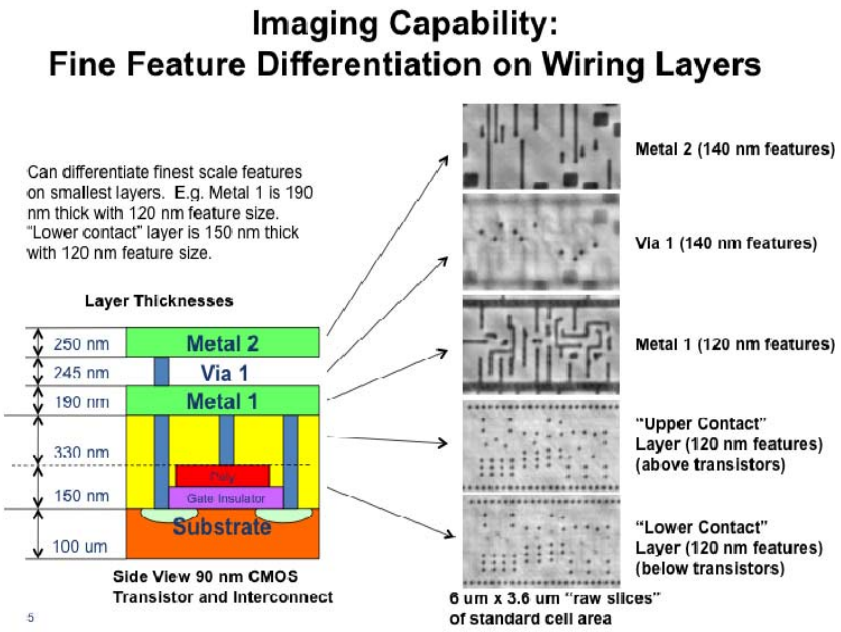

Figure 2. Layer Imaging Detail: High quality images of IC layers are formed by slicing the 3D data volume. The contact layer is resolved into substrate and poly-contacts, and the metal layers clearly indicate circuitry. Figure adapted from Bajura *et al.* (2011).

In summary, the use of x-ray nanotomography for imaging of electronic circuits, on a scale of high automation and accuracy, could enable high-throughput screening of IC chips used in critical applications in which failure could compromise critical capabilities or information. Imaging results from this project have been published in the *Proceedings of the 36th GOMACTech Conference*.

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