Machine Protection System

- Requirements
- Architecture
  - Link Processor
  - Link Node
- Timing
Requirements

- Switch off beam within one pulse at 120 Hz
  - Gun laser shutters (Mechanical and Pockels Cell) and
  - LTU single bunch beam dumper
- Distributed fault inputs along the machine
  - Primary: Beam loss monitors, toroids, obstructions
  - Secondary: PVs indicating power supply status, BPMs
Link Processor

- Determines maximum allowed beam rate
- Private GbE fiber network for MPS data
- Controls network for EPICS
- Interfaces to the LCLS timing system
  - MPS->EVG via MPS private network
  - EVG->MPS via PMC EVR
- Motorola MVME 6100 and PMC-EVR-200
MPS Link Processor

Motorola
MVME6100

Micro-Research
PMC-EVR-200
Link Node

- Units distributed along the machine
  - Fast dedicated connection to Link Processor
- Acquires fault status from BLMs and other devices
- Outputs signals to mitigation devices—injector laser shutters and LTU kicker magnet
- Slower EPICS interface for control and device status
Link Node

- Xilinx Virtex-4 FX20 FPGA
  - Interface to IndustryPack, digital input and output cards
  - Communication with MPS Link Processor over Gb Ethernet

- Arcturus ColdFire Processor
  - SLAC supported RTEMS/EPICS
  - Remote diagnostics and configuration of FPGA only
  - Reports detailed fault information to users
Link Node

- Digital Input and Output Cards
  - Inputs for device faults and status
  - Outputs for device control
- IndustryPack Bus Interface
MPS Link Node

Output Card

IP Card

Interface Board Slots

L-Board

Input Card

Trigger I/O
Link Node Functional Block Diagram

- **Coldfire Computer (RTEMS/EPICS)**
- **USB Ifc**
- **SFP**
- **FPGA**
  - **Vitrex-4 XC4VFX20**
  - **MPS Fiber Link**
- **Interface Transceivers**
- **Input Ifc Bd 1**
  - (Opto-Isolators)
- **Output Ifc Bd**
  - (Opto-Isolators)
- **General-Purpose TTL I/O**
- **GPIO for status, ctrl, etc.**
  - (Unused Trigger I/O signals)
- **Trigger I/O**
  - 4
  - 4
  - Trigger I/O can be configured as needed
- **From EVR**
- **To other devices**
- **PC Laptop**
- **Local Debug Port**
- **Node Address Switches**
- **MPS Fiber Link**
- **Fault Inputs (96)**
- **MPS Devices**
- **Mitigation Device Outputs (8)**
- **Industry Pack Interface**
- **Industry Pack Module 1**
- **Signal Cond Board**
- **Industry Pack Module 2**
- **Signal Cond Board**
- **Industry Pack Module 3**
- **Signal Cond Board**
- **Industry Pack Module 4**
- **Signal Cond Board**

**PC Laptop**

**Coldfire Computer (RTEMS/EPICS)**

**USB Ifc**

**SFP**

**FPGA**

**Vitrex-4 XC4VFX20**

**MPS Fiber Link**

**Interface Transceivers**

**Input Ifc Bd 1**

- (Opto-Isolators)

**Output Ifc Bd**

- (Opto-Isolators)

**General-Purpose TTL I/O**

**GPIO for status, ctrl, etc.**

- (Unused Trigger I/O signals)

**Trigger I/O**

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**MPS Fiber Link**

**Fault Inputs (96)**

**MPS Devices**

**Mitigation Device Outputs (8)**

**Industry Pack Interface**

**Industry Pack Module 1**

**Signal Cond Board**

**Industry Pack Module 2**

**Signal Cond Board**

**Industry Pack Module 3**

**Signal Cond Board**

**Industry Pack Module 4**

**Signal Cond Board**
Link Node Input and Output Cards

Input Card

Output Card
Timing

EVG

8-bit MPS Data (Shared Data Bus)

8-bit Event Buffer

8-bit Event

EVR

8-bit Event

Programmable Delay

Trigger
Timing

Undulator Service Building

EVR → Link Node → Link Processor

HVPS Control and Test Pulse → PMT Signal

+12V Power Supply

BLM Interface Box (Argonne)

PMT

Up to Eight per Link Node

Undulator Hall Tunnel

HV

LED Fiber Signal