LCLS Undulator Beam loss Monitor
Preliminary Design Review

BLM Control & Readout Electronics

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Hardware Design Support
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Presentation Outline

1) MPS System Overview
2) Link Node Description
3) BLM System Overview
4) Interface to BLM Detector
5) Individual HW Descriptions
6) Schedule
7) Summary
MPS System Overview
MPS Overview
LCLS MPS System Overview

**Basic Function:** To provide a fault detection and beam rate limiting mechanism that protects critical LCLS accelerator components from excessive beam power, thereby preventing damage.

**The System:**
- The LCLS MPS System is arranged in a star topology, with one central Link Processor running the MPS algorithm and multiple Link Nodes which interface to the machine status and mitigation devices. The MPS interfaces to the LCLS Timing System and the LCLS Control System.
- The Link Nodes interface to the Link Processor via a dedicated Gigabit Ethernet fiber link with a commercial G-bit Enet Switch (Cisco xxx).
- Machine status is collected by the Link Nodes and passed to the Link Processor. The Link Processor, according to its algorithm, processes the status information and responds appropriately: sending rate limiting commands to the Timing System and activating mitigation devices.
System Interconnect

LCLS Control System

LCLS Timing System

MPS Private Ethernet Link

Timing Data Fiber

Triggered Devices

Control System Ethernet

Control System Ethernet

Enet 1

Enet 2

EVR

Gbit Enet Switch

MPS Link Node

EVR

Enet 2

Inter System Communications:
- MPS & Timing both connect to main Control system of std ethernet
- MPS Receives Timing Event Information over via EVR
- MPS Transmits rate limit commands to Timing via MPS Private Ethernet

System Interconnect Diagram
LCLS MPS System Component Details

• LCLS MPS Link Processor:
  • Implemented in a VME Crate consisting of:
    • MVME-6100 CPU running RTEMS & EPICS
      • Implements MPS Algorithm
      • Interfaces to EPICS Control System via Ethernet
      • Interfaces to Link Node
      • Interfaces for Timing System Event Generator
    • MRF PMC-EVR
      • Interface to LCLS Timing System / Receives timing event data

• LCLS MPS Link Node
  • SLAC Custom-Designed Chassis (described next)
MPS Link Node Description
MPS Link Node

- The Link Node is the interface between the Link Processor and the Machine devices (sensors, valves, etc.)
- Custom Designed by SLAC LCLS Controls Group
- Implemented in a 3U, 19-inch rack-mount chassis
- Contains digital logic for status signal processing and conditioning, local processor for EPICS interface, flexible I/O including both digital and analog
- Modular design: consists of main motherboard with MPS device I/O interface boards and general-purpose interface (Industry Pack) bus
MPS Link Node - Details

- Xilinx Virtex-4 FX20 FPGA
  - Interface to IndustryPack, digital input and output cards
  - Communication with MPS Link Processor over Gb Ethernet

- Arcturus ColdFire Processor
  - SLAC supported RTEMS/EPICS
  - Remote diagnostics and configuration of FPGA only
  - Reports detailed fault information to users

- Digital Input and Output Cards
  - Inputs for device faults and status
  - Outputs for device control

- IndustryPack Bus (IP) Interface*
Link Node Block Diagram

MPS Link Node – Functional Block Diagram
Link Node - Prototype

- Industry Pack (IP) Bus Slots
- IP Module
- Connector Slots for Interface Boards
- MPS I/O Output Board
- MPS I/O Output Board
- Link Node Motherboard
- MPS I/O Input Board
- I/O Interconnect “L” Board

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Link Node MPS I/O Cards
Link Node Development Status

• Have built prototype motherboard, MPS I/O boards and L-Board
• Motherboard is working:
  • G-Bit Ethernet Link working
  • Arcturus Local Processor & Interface Working
  • Industry Pack bus interface working
  • MPS I/O board interface & logic working
• MPS I/O Boards tested & working
• Motherboard design updated with changes & corrections → beginning PCB layout mods
• Designing new L-Board for BLM project
• Some additional FPGA gateware dev needed for BLM system
• Lots of SW development (Arcturus, EPICS, etc.) still needed
Beam Loss Monitor Readout System
BLM Readout System: Proposed Design

Design Philosophy:

- Since the BLM is going to be an MPS device, why not integrate directly into the MPS System?
- Using the Link Node Chassis with a mix of custom and COTS HW, develop a solution that can control and read out the BLM detector and provide a beam loss status signal to the LCLS MPS system as well as beam loss measurement data to the LCLS control system

- Use Link Node to
  - Generate Beam Loss Fault
  - Provide analog readouts to control system
  - Set threshold levels
  - Control PMT HV power supplies
  - Generate “heartbeat” test pulse
  - Synchronized to beam using trigger from LCLS Timing System
Use one Link Node to serve 8 LCLS Undulator sections
- Use a total of 5 Link Node chassis, which leaves 5 spare channels
- There are a total of 33 undulator segments, plus 2 more BLMs: one/ea at beginning and end
- The chassis will be located in the Undulator Service Building (B913)
- The Detector will be located on the Undulator, accompanied by an Interface Box
  - The Interface Box will contain the PMT HVPS, PMT output preamp, LED and Pulser
- Link Node Will connect directly to LCLS Control System for non-MPS readout
- Link Node will Rx a Trigger from the LCLS Timing System to initiate a measurement of the PMT signal as well as generate a system Test Signal (LED Flasher)
BLM Readout System – Major Components

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BLM System – Interconnect

• Detector:
  • Cherenkov Light (Quartz Crystal)
  • PMT Readout
  • Detector Local Support functions done by BLM Interface Box (This Review – Tony Pietryla/ANL)

• BLM Interface Box:
  • Contains HPVS for PMT
  • Preamp with pulse shaping & line driver for PMT signal
  • Test LED & Driver for general heartbeat / detector health test
BLM System – Interconnect Signals

- BLM IFC Box to Link Node Signals:
  - PMT HVPS Control (Analog-DC: 0...+5V)
  - PMT HPVS Readback (Analog-DC: 0…+5V)
  - Test Trigger Pulse (Digital: 100ns min / RS-485 Diff'I)
    - These signals are sent on twisted-pair, individually shielded wires on a multi-conductor cable with overall shield / DB-9 connectors

- PMT Signal / High-Speed Voltage Pulse / 0...+1.5V
  - Sent over LMR-400 double-shielded coax / SMA connectors

⇒ Maximum System Cable Length = 300 Feet
BLM System – Grounding & Shielding

Handling of Grounding & Shielding between boxes:

- **BLM Interface Box:**
  - Signal returns are connected to internal ground
  - Individual Pair Shields are connected to same ground
    - Returns & Shields are NOT connected to box common Gnd / but there is provision to do so
  - Overall cable Shield NOT connected at this side

- **Link Node Chassis:**
  - Control Signals Returns are connected to system ground at BLM Interface Board
  - PMT Signal Return connected to system Gnd
  - Individual Pair Signal Shields are connected to system ground thru ferrite beads / shields connections can be broken if needed (if Gnd loops are present)
  - Overall cable Shield is connected to system ground thru ferrite bead / provision to open shield if needed
BLM System HW: Link Node
Link Node HW: Implementation

- The Link Node Will Contain A mixture of COTS & custom HW to implement the BLM readout & control
  - COTS HW:
    - COTS DAC: (Acromag IP-231) for HVPS Control / 16-Channel, 16-Bits
    - COTS ADC: (Acromag IP-330A) for HVPS Readback / 16-Channel, 16-Bits
      - BOTH of these module are already in use in the LCLS Control System
  - Custom HW:
    - Custom ADC for PMT Signal Acquisition, Accumulated Dose Processing & Test Trigger Generation
    - Custom Interface Boards In Link Node for IFC between BLM Ifc Box and Link Node
    - Re-Design of Link Node L-Board to map signals between IP-Modules and BLM Interface boards
Changes / Additions To Existing Link Node Design

MPS Link Node – Functional Block Diagram
Link Node BLM Hardware

• The Individual custom components will now be described:
  ▶ BLM Interface Board
  ▶ Interconnect L-Board
  ▶ Custom IP-ADC Board
BLM Interface Board
BLM Interface Board

- Provides an electrical and mechanical interface to the BLM Interface box cables
- Plug-In board, mounts to the Interconnect L-Board
- Will serve (2) BLM Interface Boxes / (4) BLM IFC Boards per Link Node Chassis for a total of (8) BLM Channels
- Contains DB-9 & SMA Connectors / Edge Card Connector (64-pin PCI-E type) on L-Board Side
- Performs the following functions:
  - Protects & Interconnects the PMT Signal
  - Protects, Filters & Receives/Buffers the HVPS readback signal
  - Buffers/Drives the HPVS control signal
  - Drives the Test/Trigger pulse signal
BLM IFC Board – Block Diagram

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BLM IFC Board – Status

• Schematic is 90% complete
• Will begin layout prep week of 1-28-2008
• Layout will take approx. 1 week
• No long-lead components
• Prototype testing to start Mid-Feb 2008
Interconnect L-Board
Link Node Interconnect L-Board

- Provides an interconnect medium between the IP Module’s I/O signals and the BLM Interface board /
- Can be thought of as a kind of “backplane” for Link Node boards
- Also contains power connector and trigger connectors
- Ties together and routes all of the I/O signals to their appropriate destinations
- Very simple, flexible design / consists of mainly connectors and traces
- Critical signals (analog & digital) are routed away from each other / copious use of Gnd planes / power filtering done at pwr entry point
- PMT signals are routed as 50Ω stripline traces
Interconnect L-Board – Block Diagram

LinkNode Interconnect L-Board
Interconnect L-Board -- Status

- Schematic started, 10% complete
- Will begin layout 2-20-2008
- Layout will take approx. 1 week
- No long-lead components
- PCB Design is part of Link Node Design File / Will be submitted with Link Node for Fab / late-Feb 2008
- Some Link Node Chassis are currently being fabricated without the L-Board.
Custom IP-ADC
Custom IP-ADC

• Plug-In, general-purpose interface board, (Industry Pack)
• Serves (8) BLM or PIC Channels
• Contains two 16 bit ADCs, each with 6 simultaneously sampled inputs. (4 spare channels are use monitor on board voltages)
• Has a gated integrator on each input to directly process a PMT or PIC Signal
• All logic is contained in a xilinx spartan 3. The xilinx sets digital trip thresholds and digital filtering of signals
• Contains two 50 pin SSCI Connectors one for analog input and one for the IP bus interface
• Mounts between the Interconnect L-Board and the main Link Node board.
• Sources a LED Test/Trigger pulse signal
CUSTOM IP-ADC (BLM OPERATION)

Available DATA

• This card consists of 8 gated integrators followed by an 8 channel simultaneously sampling ADC.
• Six analog values are measured and are available for readout for each channel.
  • The charge ($Q_p$) for the last pulse.
  • The charge ($Q_{60}$) accumulated for the last 1/60 Second
  • The charge ($Q_{30}$) accumulated for the last 1/30 Second
  • The charge ($Q_{10}$) accumulated for the last 1/10 Second
  • The charge ($Q_1$) accumulated for the last 1Sec.
  • The test charge ($Q_t$) for the last led pulse cycle.
CUSTOM IP-ADC (BLM OPERATION)

Trip Thresholds

- There are four programmable thresholds levels for each channel.
  - There are two 16 bit values tested against the digitized and accumulated charges for each channel
    - 10 fault conditions
  - There are two 16 bit values tested against the digitized test charge. A lower limit threshold and a high limit threshold.
    - 2 fault conditions

- Fault Registers one for each Channel (x)
  - B0 CH_x_Qp_0 Fault
  - B1 CH_x_Qp_1 Fault
  - B2 CH_x_Q60_0 Fault
  - B3 CH_x_Q60_1 Fault
  - B4 CH_x_Q30_0 Fault
  - B5 CH_x_Q30_1 Fault
  - B6 CH_x_Q10_0 Fault
  - B7 CH_x_Q10_1 Fault
  - B6 CH_x_Q1_0 Fault
  - B7 CH_x_Q1_1 Fault
  - B8 CH_x_Qt_L Fault
  - B9 CH_x_Qt_H Fault
CUSTOM IP-ADC (BLM OPERATION)

• Trigger Input
  • The external trigger starts a 20 uSec Integration Gate. This Trigger time is about about 10 uSec before beam time. At the end of the gate interval the Track and Holds on all 8 ADC channels are set to “Hold”. All channels are then digitized and the integrators are placed in reset mode for 1 mSec. Then a second 20 uSec gate and digitization cycle takes place. The second digitization is used for base-line or pedestal subtraction. The trigger rate for the BLM will always be 360pps. On every twelfth base-line cycle the LEDs will be pulsed and the value digitized for comparison against a trip threshold.
CUSTOM IP-ADC (BLM OPERATION)

BLM Timing

The proposed trigger timing for the BLM System will be derived from 119MHz with Fiducial (i.e. nominal Fido signal)

![119 MHz Fiducial Timing Diagram](image)

The MPS Link chassis will receive this signal on a trigger input and will output a trigger for the BLM approximately 1020 usec after the fiducial.

FIDUCIAL

INTEGRATION WINDOW = 20uSec

BEAM

Base-line Test window 20uSec
CUSTOM IP-ADC

Averaging Fault Trip Logic

ADC DATA

DIVIDE BY 330

1 Second Average

BASE LINE DATA

330 Word Shift Register

Q330

BL CLK

UPDATE CLK

D1

Q1

360 Word Shift Register

Q36

Q360

Fault Outputs

Comparators

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Operation:  120 Hz 0.8% Loss / Pulse

SystemView

1 Sec Integ (t17)

0 500e-3 1.5 2

Amplitude

Time in Seconds

SystemView

0.1 Sec Integ (t22)

0 500e-3 1.5 2

Amplitude

Time in Seconds
Operation: 1 Hz 96% Loss / Pulse
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Notes:
1. (1) Load these resistors to activate charge integration
2. (2) Load these resistors when charge integration is not required
3. The charge integration capacitor C1 is a 100pF for the BLM application and 10,000pF for the PIC.

Block Diagram for the Custom BLM ADC Board
Shaping Amplifier Response
CUSTOM IP-ADC STATUS

• Schematic almost completed, 98% complete
• Will begin layout prep week of 2-4-2008
• Layout will take approx. 2 weeks
• No long-lead components
• Xilinx code just started, 10%
• First production unit should arrive 3 -10 – 2008
  • Xilinx code needs to be ready at that time.