

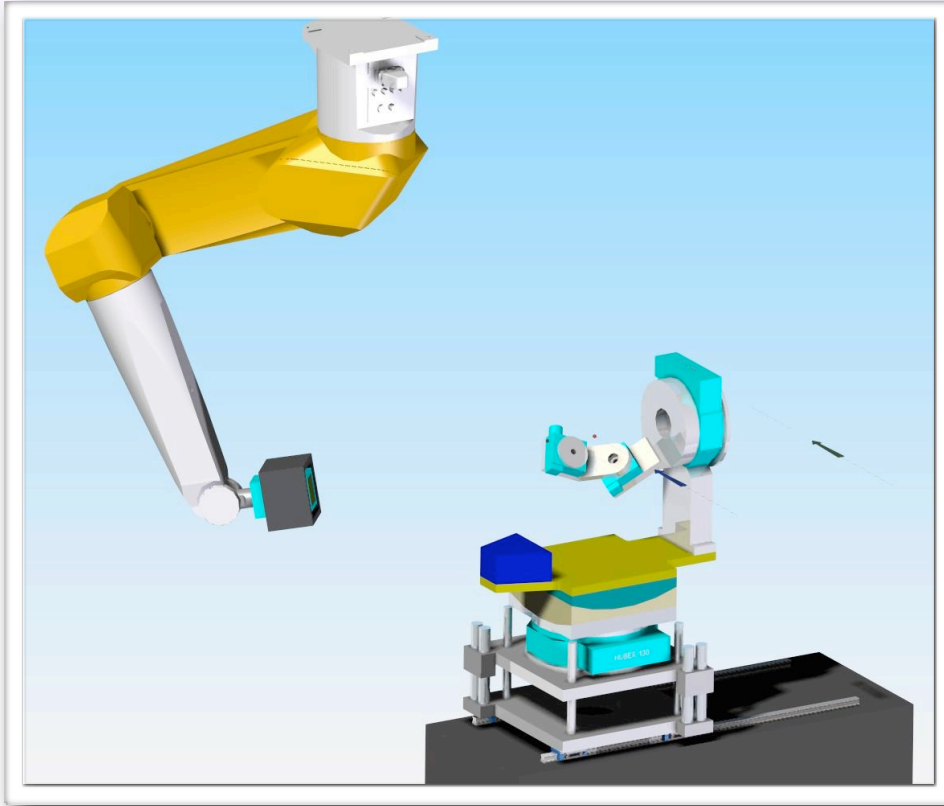
- **Detector program**
- **XPP detector**
 - Requirements, Technical, Schedule, Status & Budget
- **XCS detector**
 - Requirements, Technical, Schedule, Status & Budget
- **CXI detector**
 - Requirements, Status
- **DAQ**
- **Summary & Outlook**



- Intense (10^{12} ph) and short (100 fs) pulses at 120 Hz need integrating detectors with fast readout (< 8 ms)
- Detector specs, what will be available for LUSI

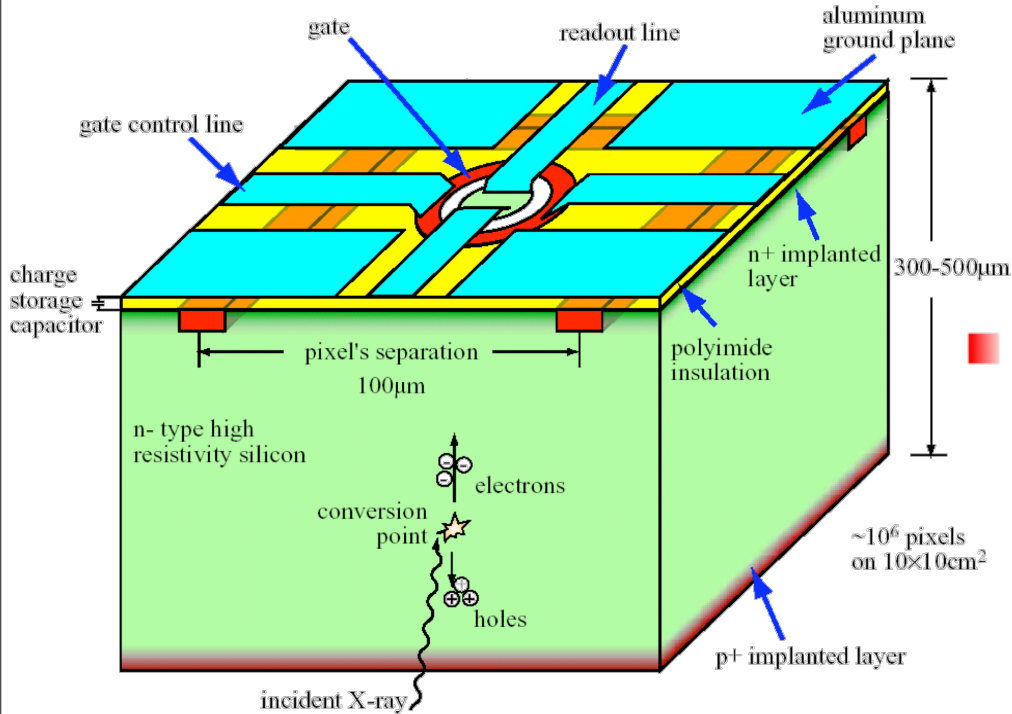
	CXI	XPP	XCS
Readout noise	< 0.3 ph	<1 ph	<<1 ph
Full well capacity	1- 10^3 ph	1- 10^4 ph	1-100 ph
Pixel size	110 μm	90 μm	≤ 35 μm
Number of pixels	760 ² (1500²)	1024 ² .	1024 ² .

- Active thickness of commercial CCDs (1-50 μm) gives poor quantum efficiency
- Pixel sizes $< 20 \mu\text{m}$ for standard CCDs
 - Small area devices or heavy tiling
 - Charge sharing works against 'photon counting'
- Best commercial CCDs have full-well of $\sim 500,000$ electrons
 - One 8 keV photon generates 2200 electron-hole pairs \rightarrow about 200 photons max full well.
 - Spec. up to 10^4
- Readout of commercial devices not fast enough
 - Millisecond readout requires highly parallel readout structure



- Pixel sensor
- Readout ASIC
- DAQ
- Mechanical design

- A sample is ‘pumped’ to an excited state by a pump pulse (e.g. laser) and analyzed after Δt with an LCLS pulse. Image the scattering intensity that is slowly varying with scattering angle (in steps) or a number of Bragg peaks.
 - High QE to achieve enough counting statistical accuracy to capture the relative intensities that resolve the induced structural changes.
 - Total angular coverage of $2\theta = 180^\circ$ to measure changes down to Ångstrom length scales
 - Angular resolution or pixel size: Bragg peaks on the detector mainly defined by beam size on the sample. For a beam size $\leq 200 \mu\text{m}$ (FWHM), a pixel size of $90 \mu\text{m}$ and variable sample to detector distance one can resolve the Bragg peaks.
 - Number of pixels 1024×1024 to resolve up to a few 100 diffraction peaks over the detector area.
 - Read-out noise < 1 equivalent 8.2 keV photon to allow single photon sensitivity



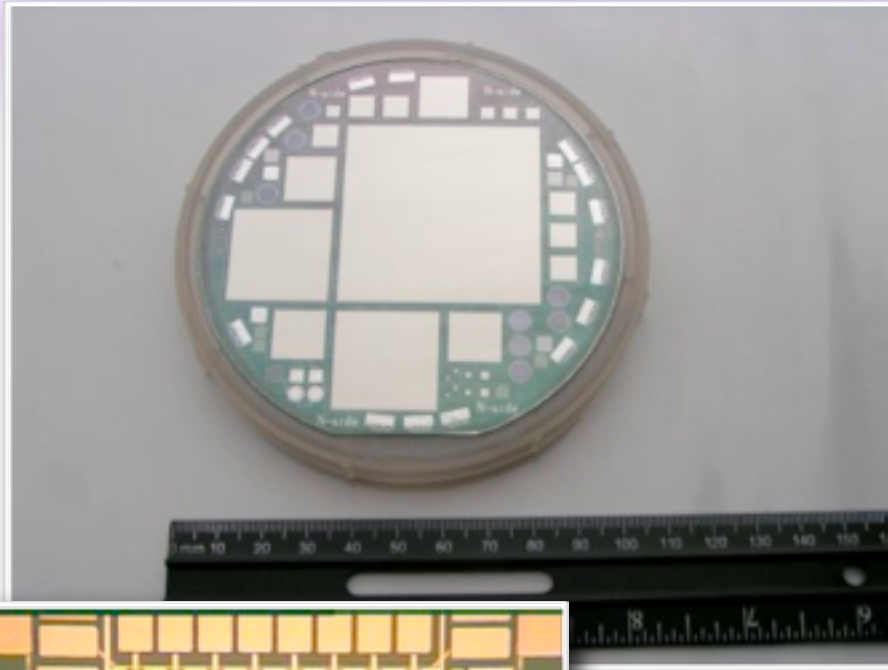
Switch-matrix structure for XPP experiments

During data accumulation each row of pixels is switched on and the pixel charge is readout

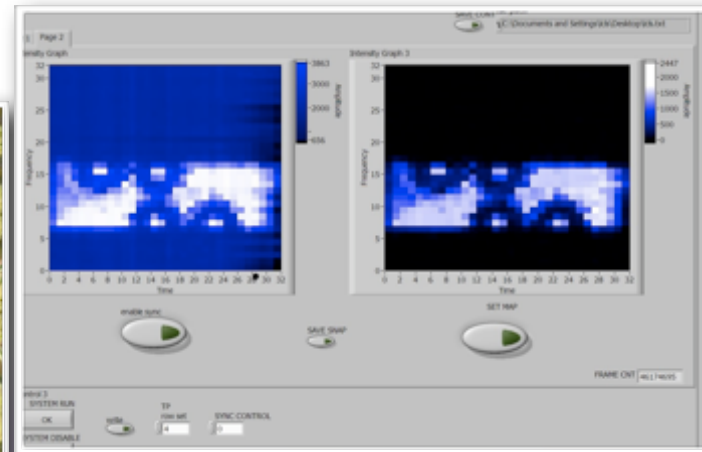
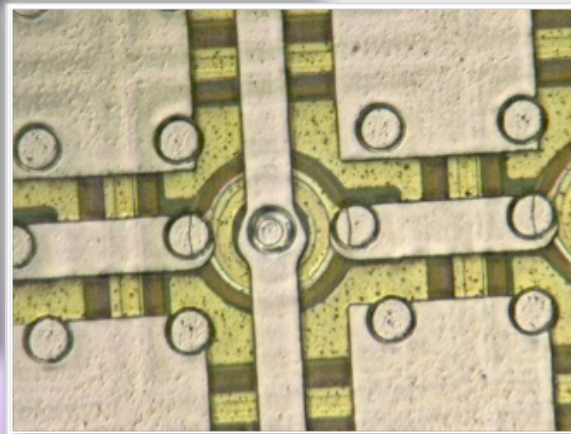
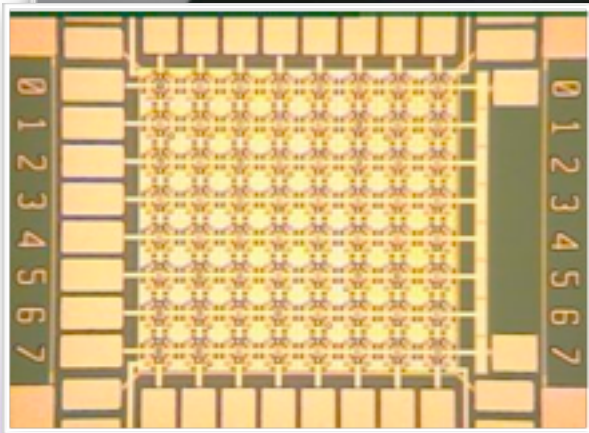
- Extremely challenging spec: $>10^4$ S/N, single-shot, fast readout

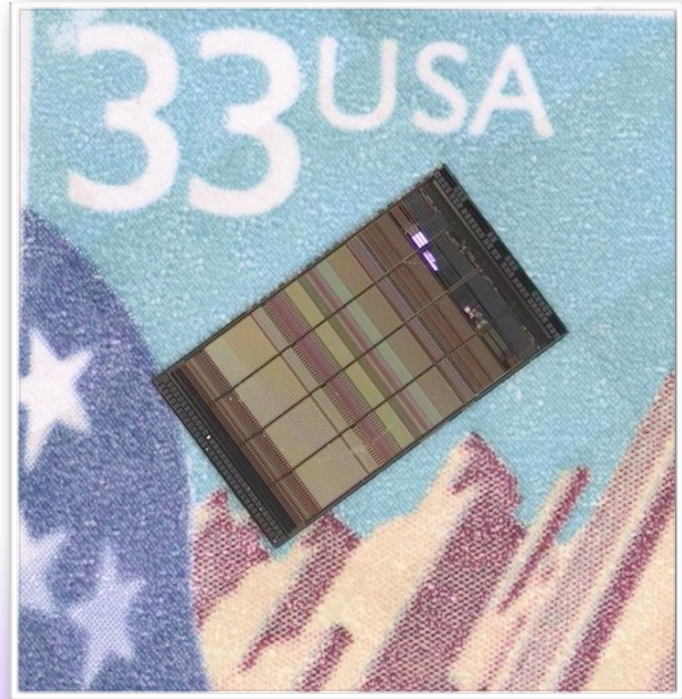
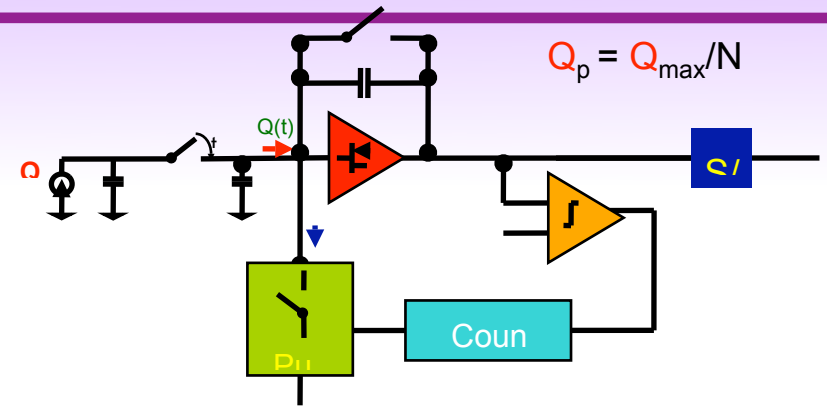
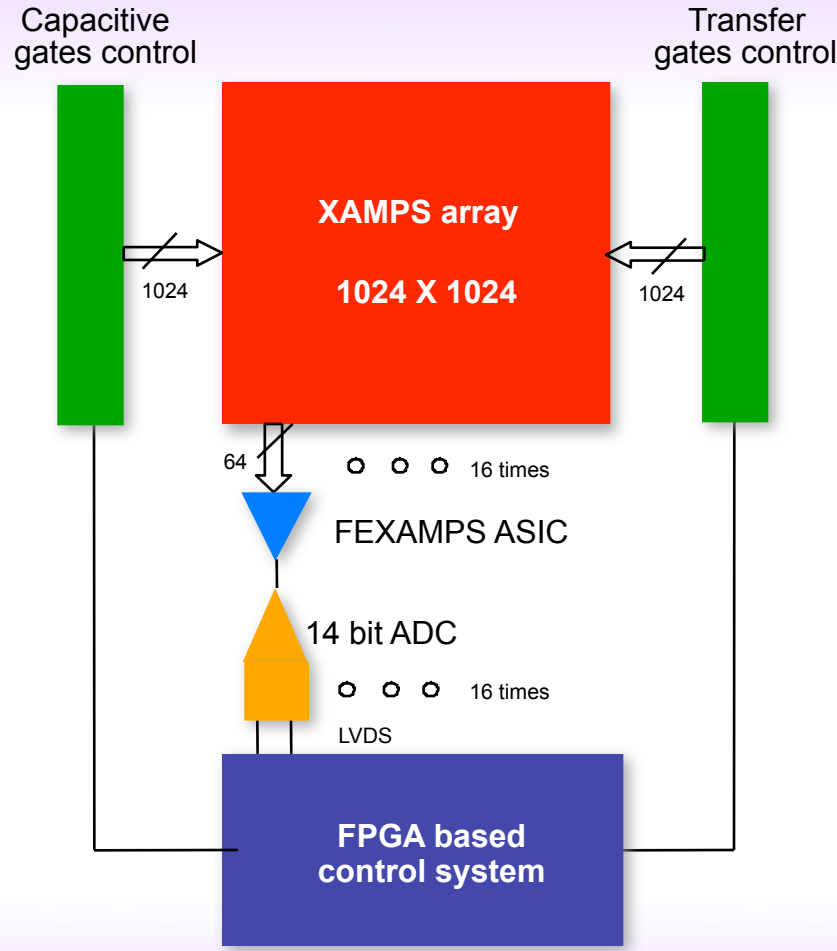
XAMPS

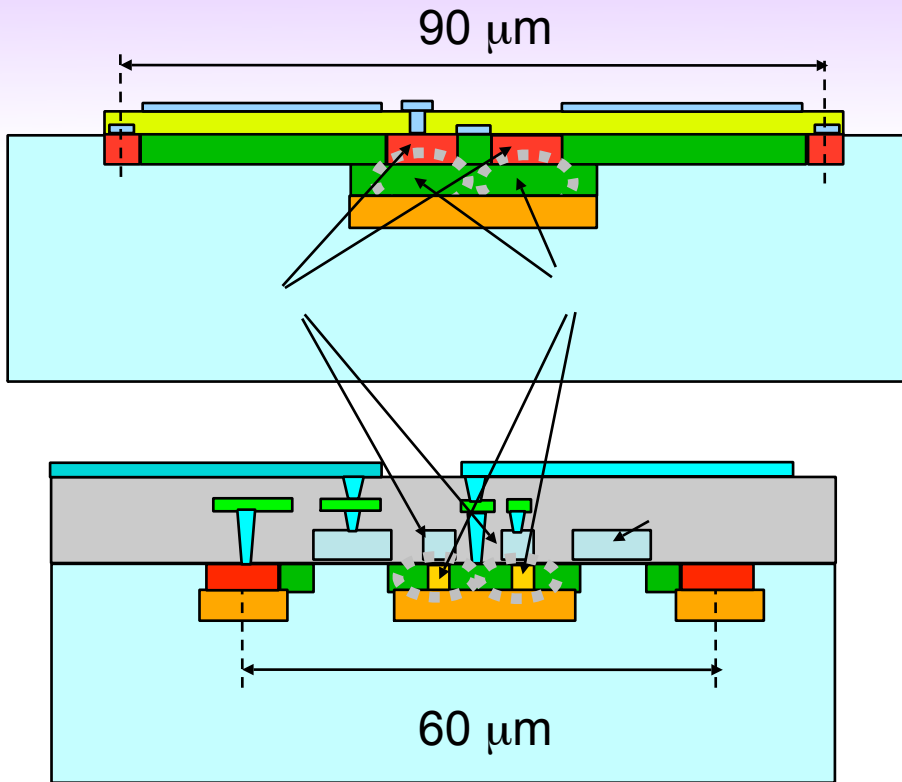
- Monolithic devices built on silicon provide simplest structure
- Need to develop technology to form transistors directly on high-resistivity Silicon substrate
- No bump-bonding and no on-pixel amplifier allows for smaller pixel size



- 512 x 512 module
 - 100 mm n-type wafer
 - 400 μm thick
- BNL in-house process
 - Vias and inter-metal layers
 - Metalization step for 150 nm
- X-rays with 32x32 module

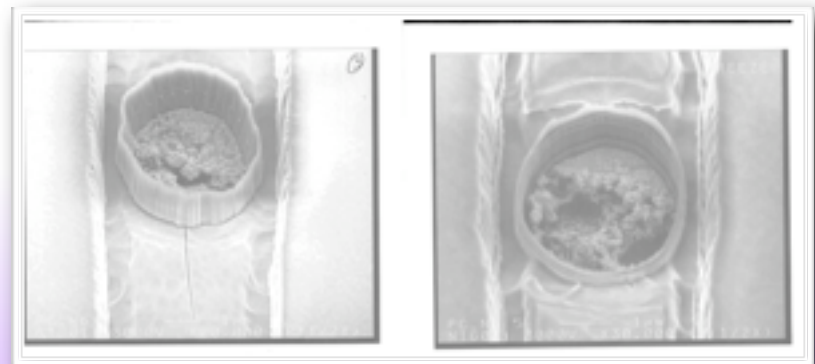


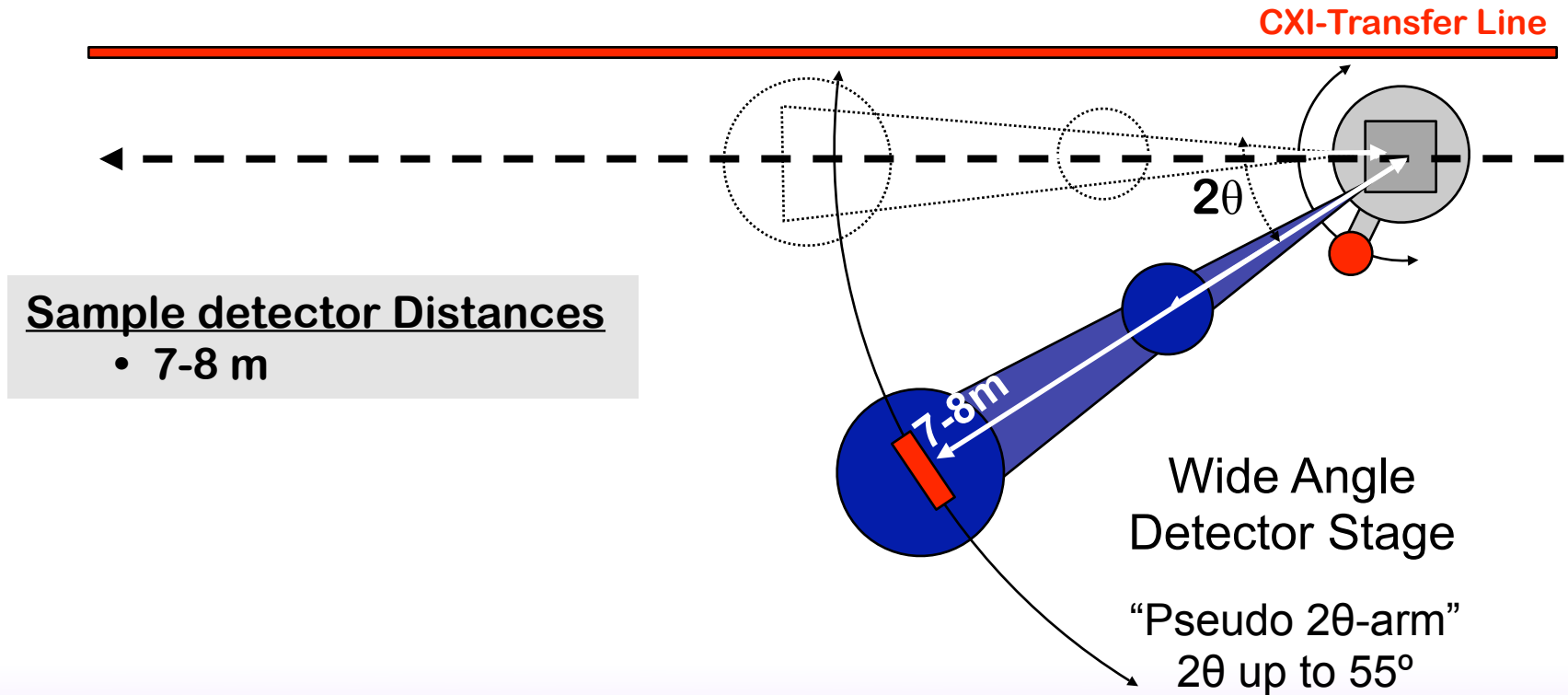




- Significant alignment and processing difficulties.
 - Veils of unknown origin cannot be etched away
 - M2 deposition not possible until this is resolved
- No pixel-side test structures were functional.
- Processing stopped until this problem resolved.

- Allows more complex circuits
- Reduce noise

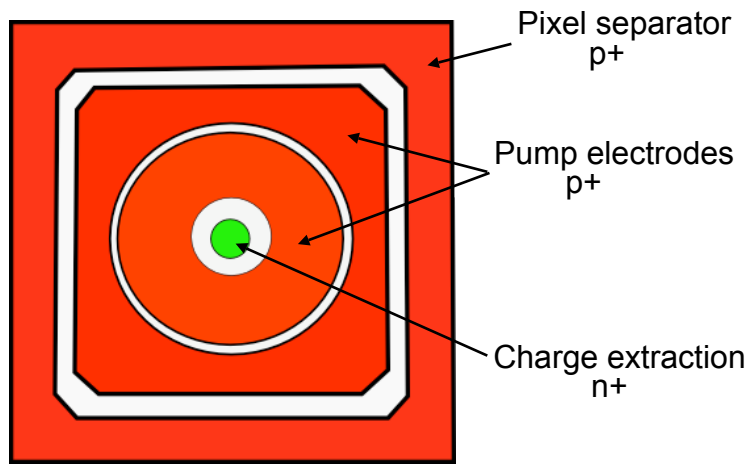




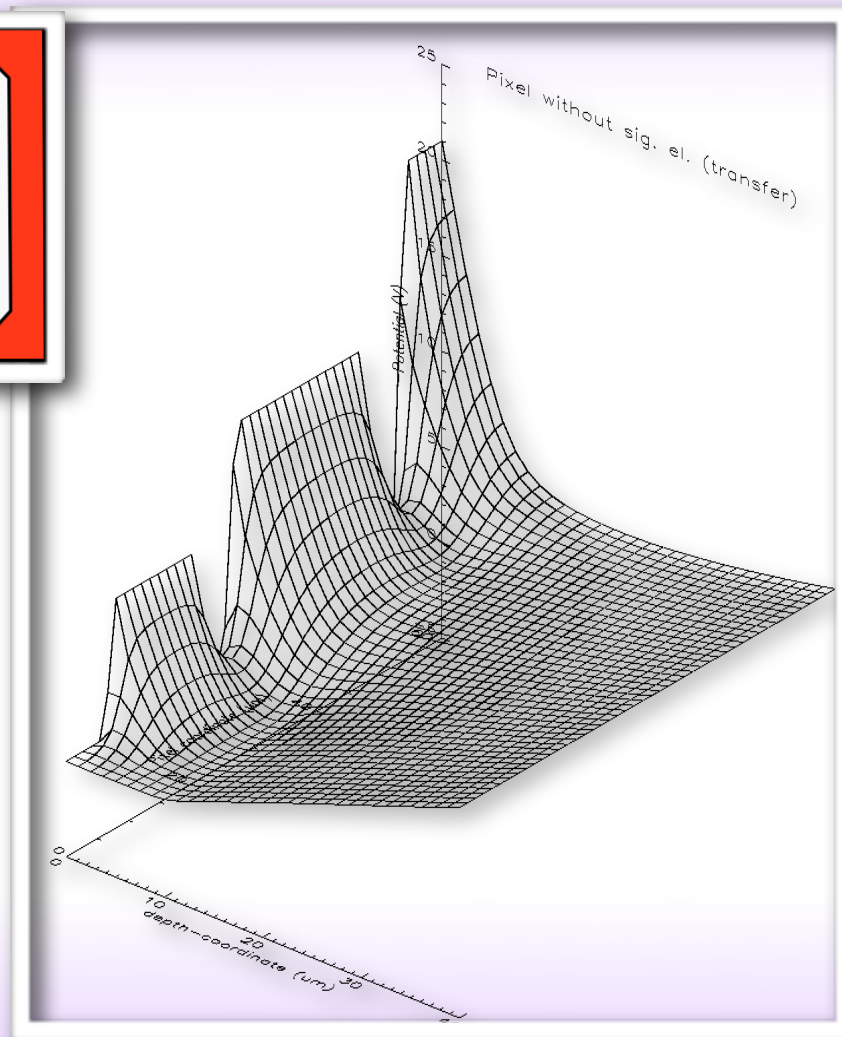
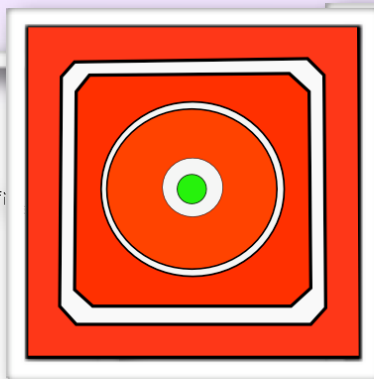
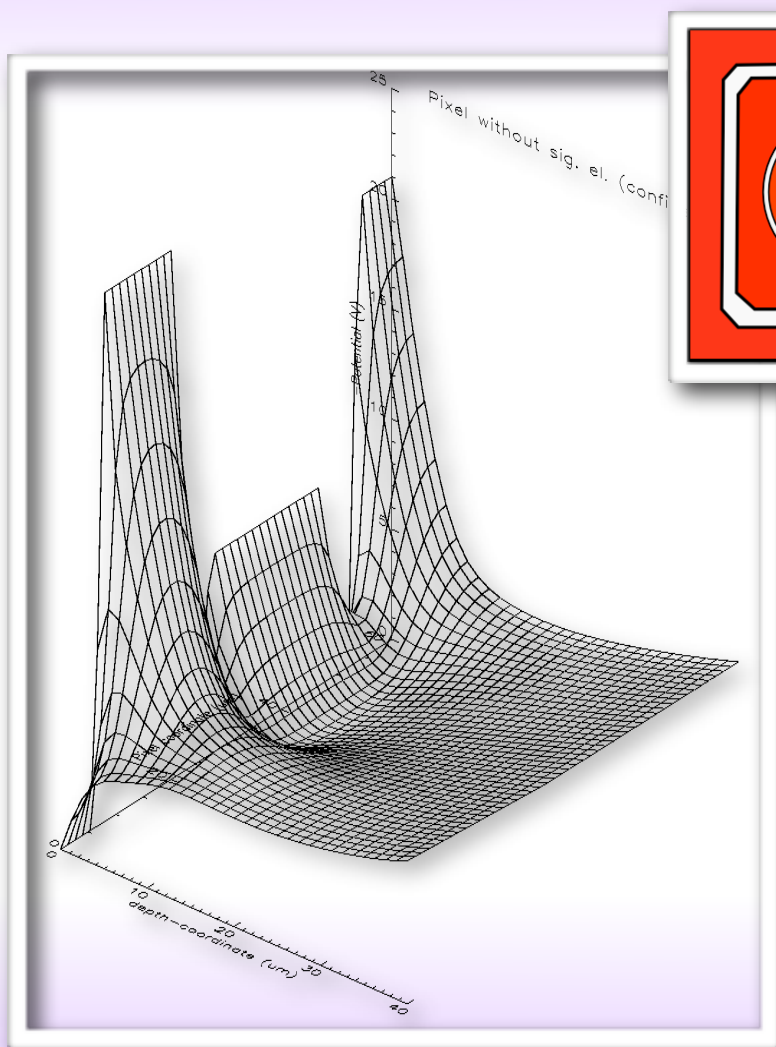
- Image the temporal changes in a speckle patterns that are related to the sample's dynamics. The method takes advantage of the coherence properties of the beam.
 - Energy range 4 - 25 keV
 - Need a high QE (> 90%) to measure the spiky nature of the speckle pattern
 - Total angular range is $2\theta = 55^\circ$
 - The detector size is determined by the maximum Q value achievable in the small angle regime
 - Angular resolution or pixel size: the pixel size should be \leq speckle size
 - For $L = 7 - 8$ m, $D_b = 10 - 100$ μm the speckle size $D_s = 11 - 120$ μm (@ 8 keV)
 - Number of pixels calculated by the total angular coverage and angular resolution needed for SAXS @ 8m. The basic detector module has 1024 x 1024 pixels
 - Read-out noise \ll 1 equivalent 8.2 keV photon to allow single photon sensitivity

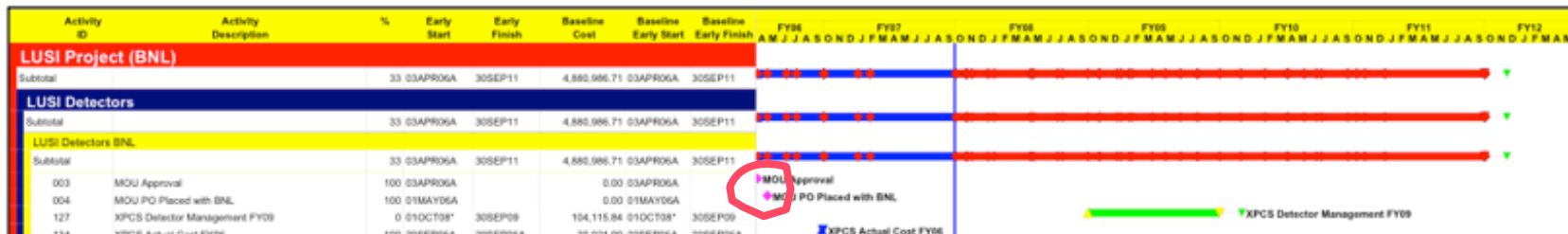
■ “Charge-pump” structure for XCS experiments

Charge is stored in a potential well and released in a controlled way similar to a drift detector

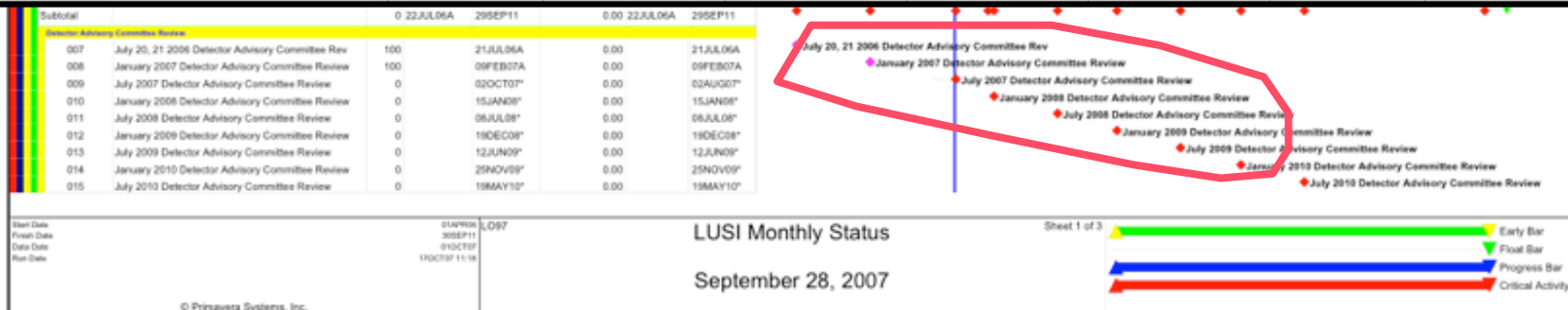


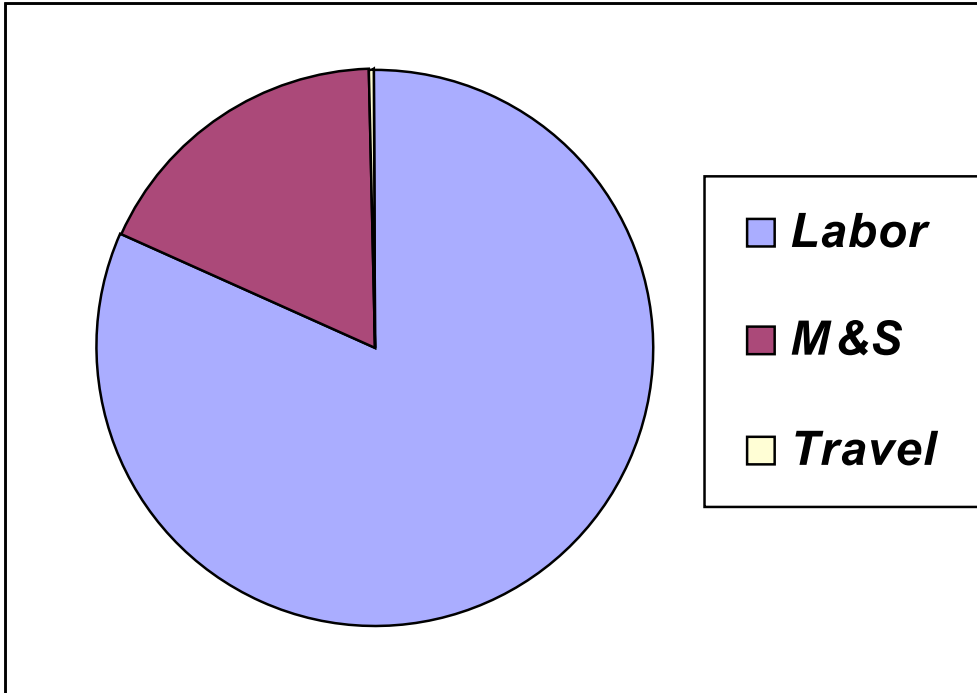
- $\ll 1$ photon readout noise, needs different technology without transistor switch
- Means that small pixels are possible.
- No “kTC noise”





WBS	CY07	CY08	CY09	CY10	CY11	CY12	Cumulative
Niels van Bakel							
1.2.04 XPP Detector System (BNL)	\$ 19,201	\$ 748,307	\$ 511,590	\$ 9,230	\$ -	\$ -	\$ 1,288,328
1.4.03 XCS Detector System (BNL)	\$ -	\$ 362,415	\$ 633,474	\$ 687,401	\$ 204,417	\$ -	\$ 1,887,707
CAM Totals:	\$ 19,201	\$ 1,110,722	\$ 1,145,063	\$ 696,631	\$ 204,417	\$ -	\$ 3,176,035





CAM - van Bakel	
Resource Type	Value
Labor	\$2,593,610
M&S	\$572,505
Travel	\$9,920
Total BAC	\$3,176,035

Including OPC: BAC = \$4.8M

■ MOU May 2006

- Technical Addendum C ends September 30 2008

■ L4 Milestones achieved

- LDAC reviews (5) and progress reports (2)
- XPP Design and fabricate **test pixels**, Sept 07, \$418k
- XPP Tested **Controls and DAQ** interface, Nov 2007, \$76k
- XPP ASIC design **computer interface**, Nov 2007, \$268k
- XPP **Prototype sensor** test & characterization, May 07, \$219k
- XPP ASIC integration with **computer system**, Jan 08, \$134k
- XPP **ASIC design**, April 08, \$147k
- XPP **pixel design** finalized, May 08, \$96k
- XPP Fabricate **IBM pixel**, May 08, \$138k
- XPP **ASIC fabrication**, June 08, \$40k

■ Current activities: ASIC and 512 sensor testing (IBM)

- XPP Design Finalized Aug, 08
- XPP Detector Delivered to SLAC Jan, 10
- XPP Installation at SLAC Complete Nov, 10
- CD-4a July, 10
- XCS Design Finalized July, 11
- XCS Detector Delivered to SLAC Nov, 11
- XCS Installation at SLAC Complete Dec, 11
- Closeout Review Nov, 11
- CD-4c April, 12

- **Technical Addendum-A (4/1/06-9/30/06, \$537k):**
 - Complete detailed XPP detector architecture design
 - Design and begin fabrication of small prototypes of the fundamental pixel elements
 - Identify possible approaches for the XCS detector
 - First pass at computer architecture design complete
- **TA-B (10/1/06-9/30/07, \$1,214k):**
 - First silicon of XPP pixels in hand and tested
 - Working XPP pixel prototypes fully tested and characterized
 - XPP ASIC design complete and submitted for fabrication
 - Design of XPP ASIC-DAQ interface complete
- **TA-C (1/1/08-9/30/08, \$779k):**
 - Design XPP detector finalized and fabrication of large area array begun.
 - Integration of pixel arrays with ASIC
 - Integration of ASIC with DAQ

1.2 XPP Instrument

1.2.01	XPP System Integration & Design
1.2.02	XPP X-ray Optics & Support Table
1.2.03	XPP Laser System
1.2.04	Detector
1.2.05	XPP Sample Environment & Diffractometer System
1.2.06	XPP Facilities
1.2.07	XPP Vacuum System
1.2.08	XPP Installation

1.3 CXI Instrument

1.3.01	CXI System Integration & Design
1.3.02	CXI X-ray Optics
1.3.03	CXI Lasers
1.3.04	CXI Coherent Imaging Injector
1.3.05	CXI Sample Environment
1.3.06	CXI Hutch Facilities
1.3.07	CXI Vacuum System
1.3.08	CXI Installation

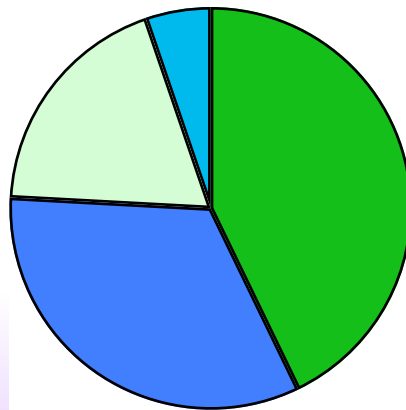
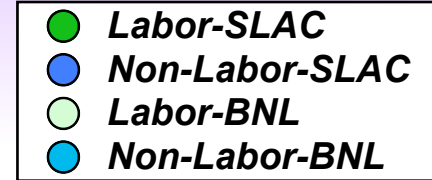
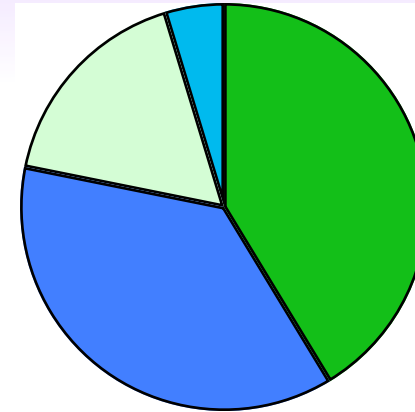
1.4 XCS Instrument

1.4.01	XCS System Integration & Design
1.4.02	XCS X-ray Optics & Support Table
1.4.03	Detector
1.4.04	XCS Sample Environment & Diffractometer System
1.4.05	XCS Hutch Facilities
1.4.06	XCS Vacuum System
1.4.07	XCS Installation

WBS	FY07	FY08	FY09	FY10	FY11	FY12	Cumulative
1.2.04 Detector	\$ 0	\$ 727,502	\$ 698,306	\$ 26,032	\$ 16,053	\$ 0	\$ 1,467,893
1.4.03 Detector	\$ 0	\$ 0	\$ 600,129	\$ 1,064,686	\$ 335,879	\$ 183	\$ 2,000,876

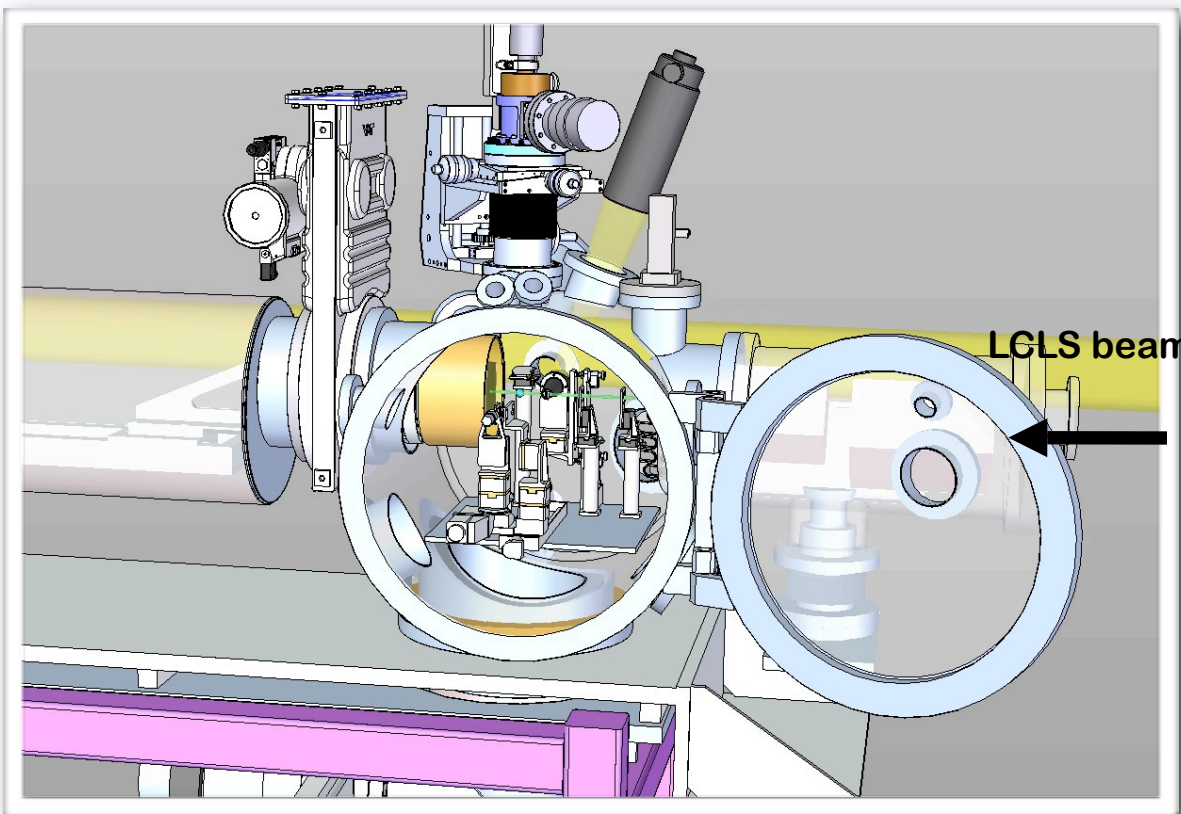
Control Account Manager	Control Accounts	Work Packages	Values
Niels van Bakel	8	9	\$3,468,769

WBS 1.2	
Resource Type	Value
Labor-SLAC	\$2,454,983
Non-Labor-SLAC	\$2,189,886
Labor-BNL	\$1,018,849
Non-Labor-BNL	\$278,767
Total BAC	\$5,942,485

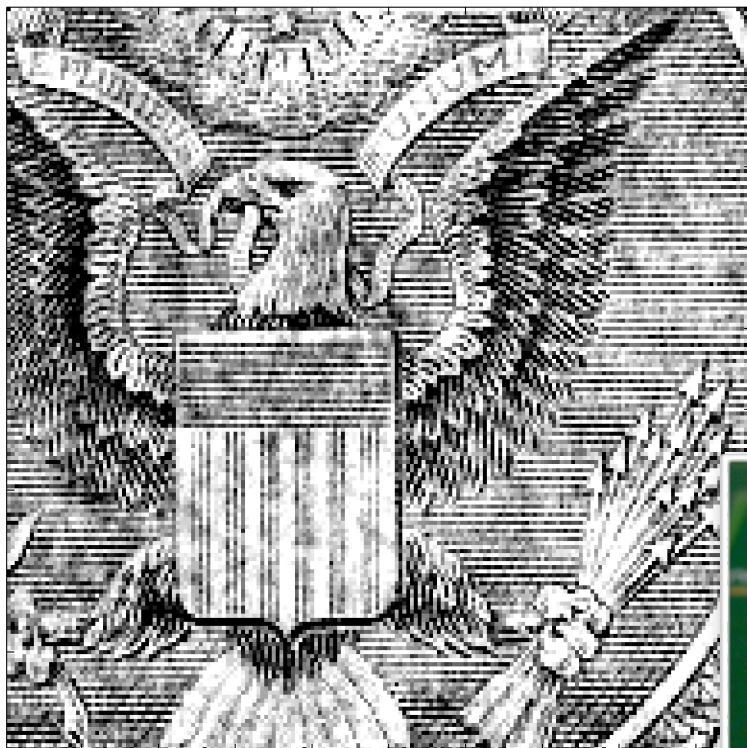


WBS 1.4	
Resource Type	Value
Labor-SLAC	\$3,303,884
Non-Labor-SLAC	\$2,548,522
Labor-BNL	\$1,457,717
Non-Labor-BNL	\$405,142
Total BAC	\$7,715,265

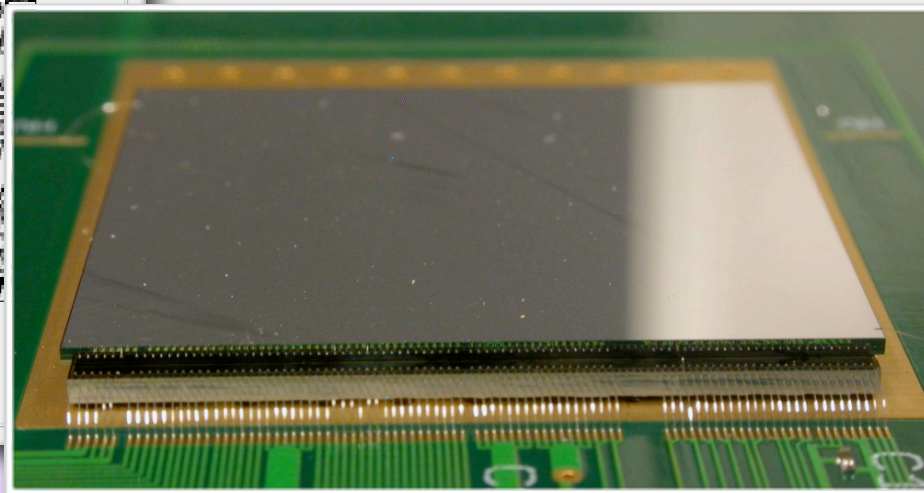
- Three subsystems: sensor elements, FE-electronics (ASIC) & DAQ
- MOU required us to assess project risks:
 - Largest risk is associated with producing essentially full-wafer devices and the possibility of vanishingly small yield
 - Attempts to identify an additional foundry led to the IBM Thomas J. Watson Research Laboratory in Yorktown Heights, NY, long-time users of NSLS
 - Discussions with IBM engineers suggested a development path which promises more than simply risk mitigation



- Detector in vacuum 10^{-7} Torr
- Resolution depends on the sample-detector distance
 - Requires translation stage 700 mm
 - Remote Aperture resizing 1 - 10 mm
- Cooling 10 - 25 °C



- Transmission Radiograph of a Dollar Bill taken with the LCLS Full Scale Prototype Module with Cu x-ray tube source, April 2008



Light shroud
(cover removed)

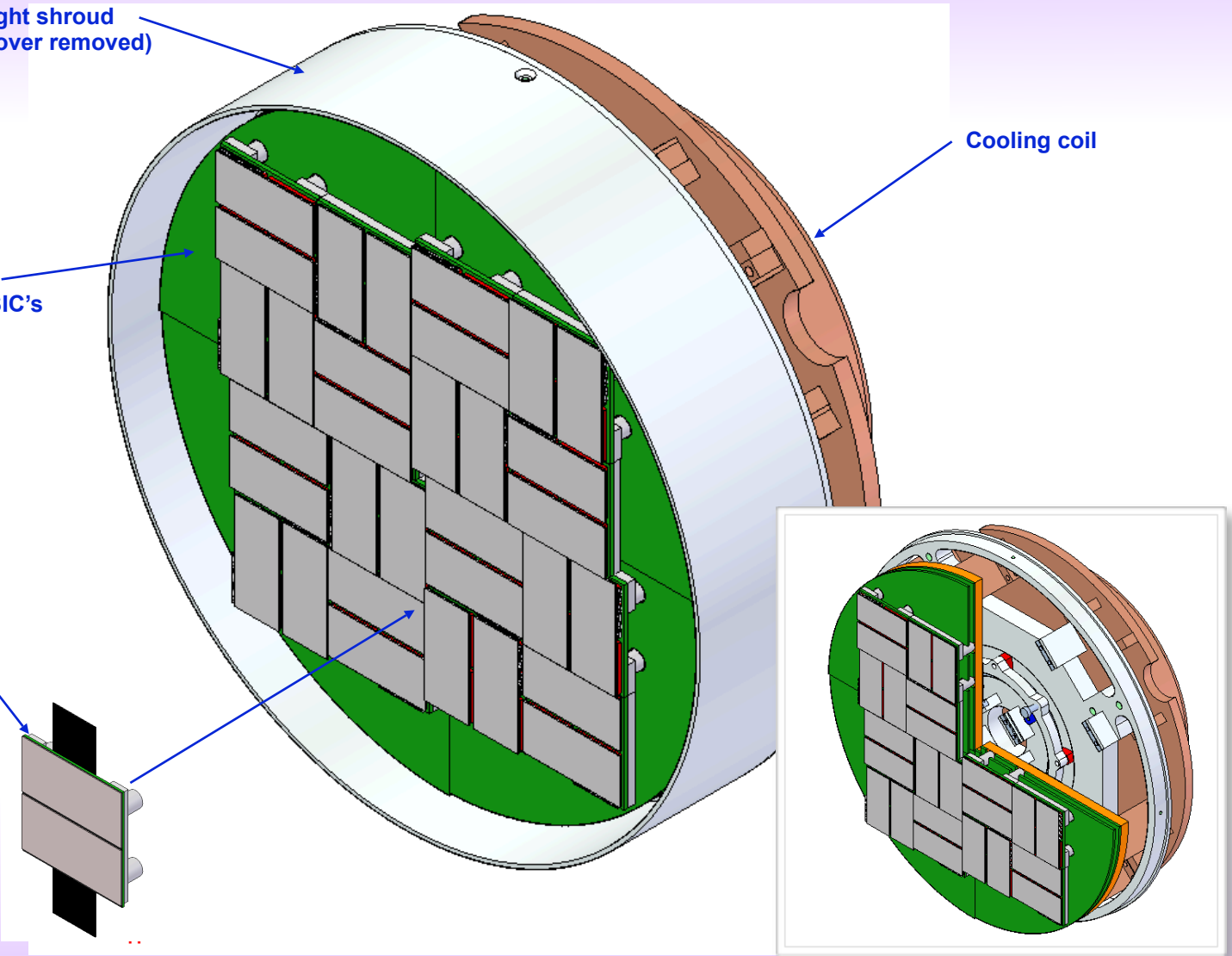
Cooling coil

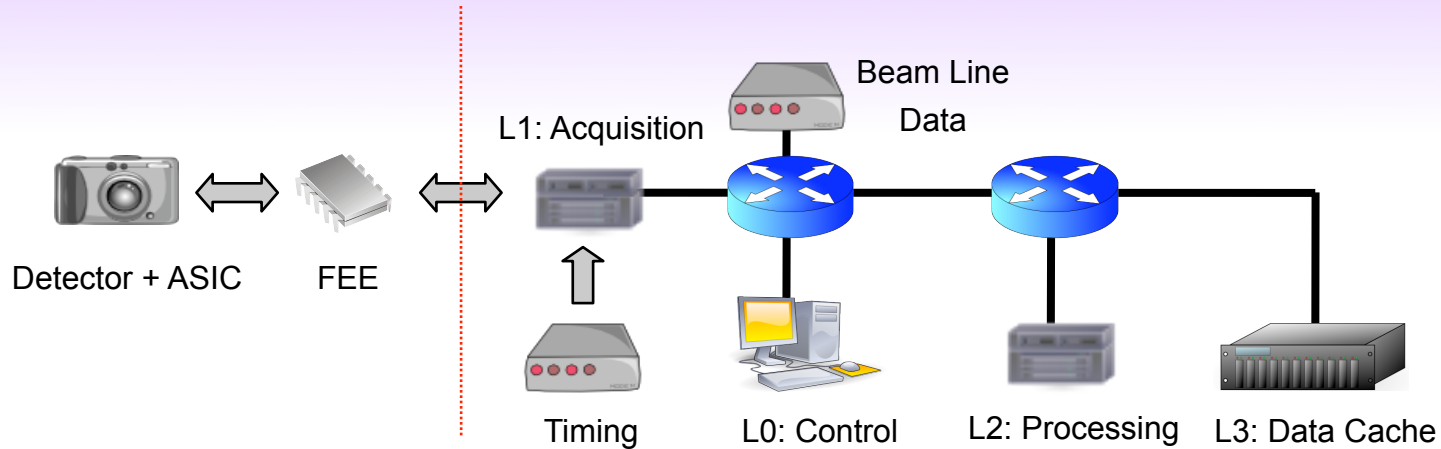
Quadrant board

- Combines signals from 16 ASIC's
- 1 FPGA/quadrant

Double detector package

- 4 ASIC's
- 2 pixel array detectors



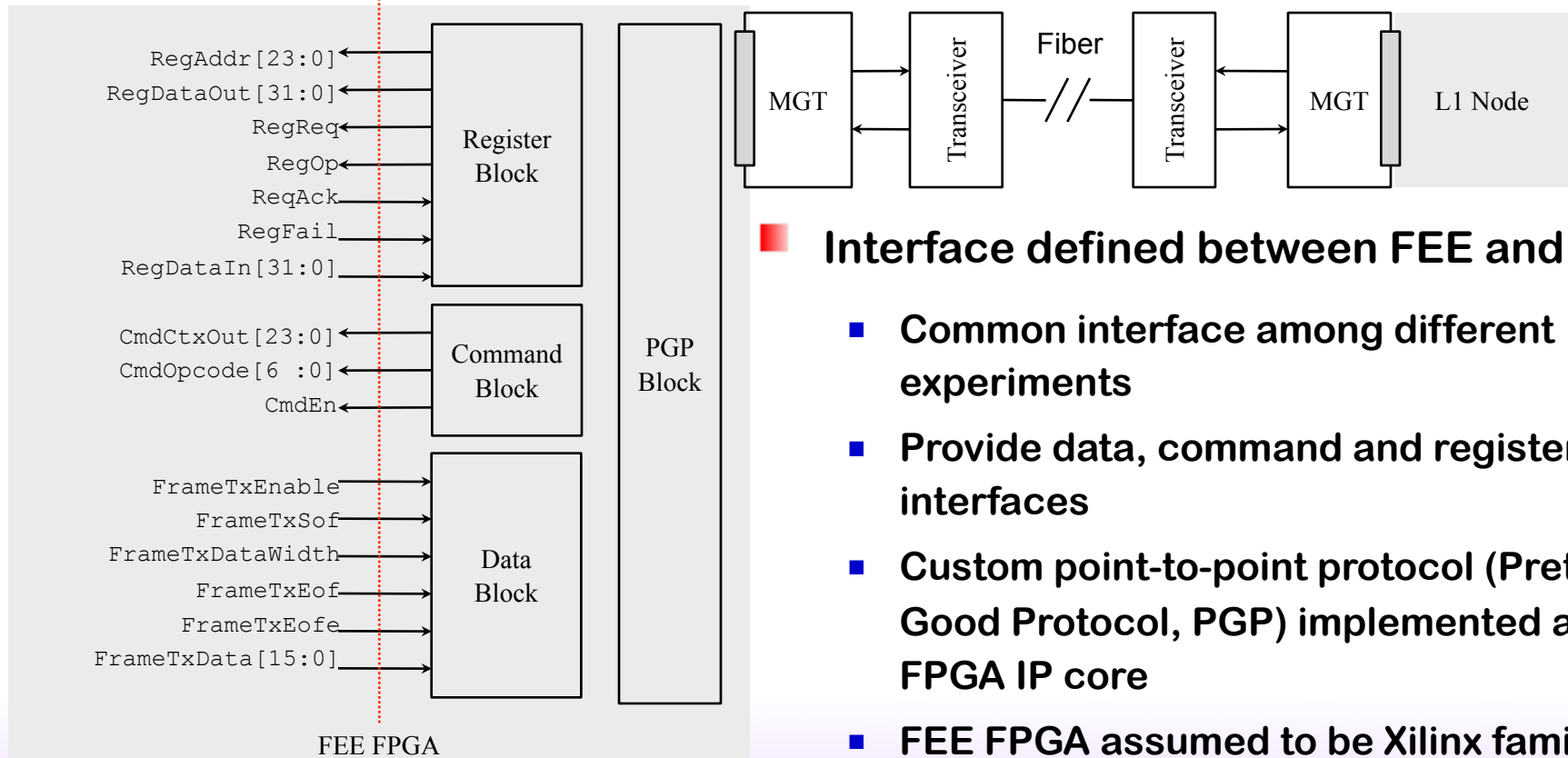


- **Detector - Experiment Specific**
- **Front-End Electronics - Local configuration registers and state machines, FPGA used to transmit to DAQ system**
- **Timing info from the accelerator timing system, distributed to the detectors and L1 boards**
- **L0: DAQ operator consoles, control a run & configure the detector, telemetry monitoring**
- **L1: Acquire FEE data, detector calibration, event building, image processing, 10 Gb/s ethernet**

Register Command Data Interface

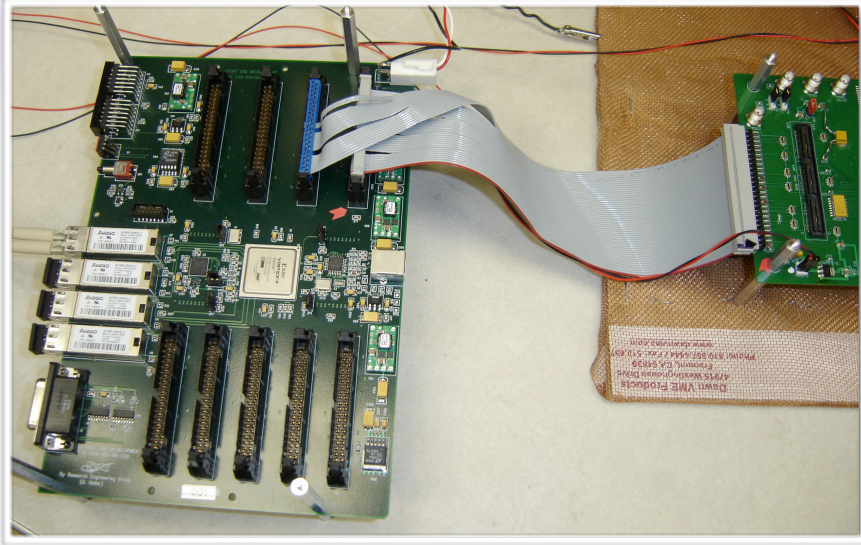
Detector specific blocks

PCDS blocks

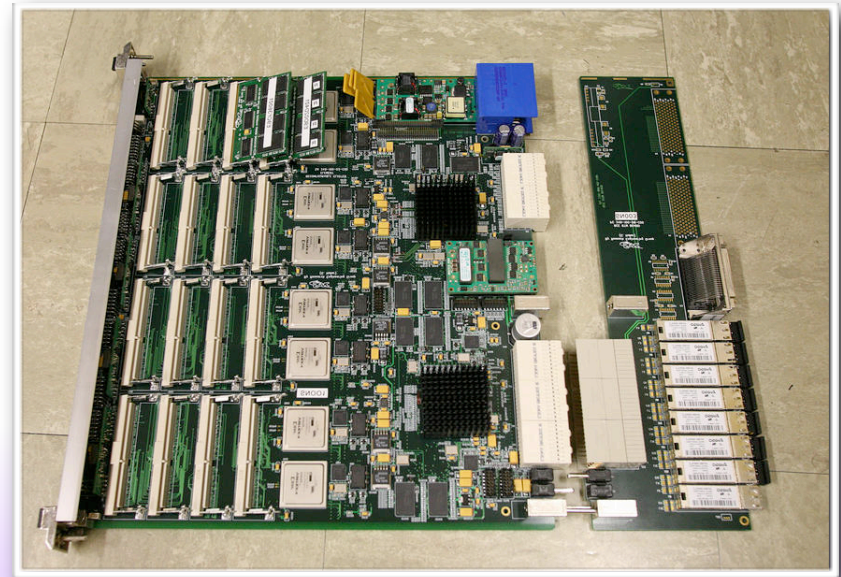


Interface defined between FEE and L1

- Common interface among different experiments
- Provide data, command and register interfaces
- Custom point-to-point protocol (Pretty Good Protocol, PGP) implemented as FPGA IP core
- FEE FPGA assumed to be Xilinx family with Multi Gigabit Transceivers (MGT)



- SLAC Front End Development board
- Additional testing; feedback to Cornell
- Improves integration in LCLS & LUSI instruments



- SLAC custom made ATCA board
- Based on System On Chip (SOC) Technology: Xilinx Virtex 4 (6)
- System Memory Subsystem: 512 MB of RAM, 8 GB/s throughput
- Configuration Flash Memory Subsystem: 128 MB for storing software code and configuration parameters (up to 16 images)

- Cornell 2D PAD detector ready in July 2009 => CXI ready in July 2011
- BNL XAMPS detector at SLAC October 2009 => XPP ready in July 2010
- BNL 2nd detector at SLAC October 2011 => XCS ready in April 2012

- **LCLS & LUSI Scientists**
- **BNL: Peter Siddons, Pavel Rehak, Zheng Li, Wei Chen, Gabriella Carini, Paul O'Connor, Gianluigi De Geronimo, Angelo Dragone,**
- **SLAC DAQ: Gunther Haller, Amedeo Perazzo, Mark Freytag, Mike Huffer, Chris O'Grady, Leonid Sapozhnikov, Eric Siskind, Dave Tarkington, Matt Weaver**
- **SLAC Mechanics: Martin Nordby, David Nelson, Matthew Swift**
- **SLAC Testing: Ryan Herbst, Dieter Freytag**
- **Cornell: Sol Gruner, Hugh Philipp, Mark Tate, Marianne Hromalik, Lucas Koerner**