LCLS Machine Protection System

- Outline
  - Overview of MPS
  - Interim MPS
  - LCLS MPS Design
  - Schedule
  - Task Assignment

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Requirements

- LCLS beam rate is 120 Hz
- MPS must turn off beam within one pulse (8.3 ms)
- Multiple rate limiting areas
  - Virtual Cathode
  - Injector Cathode
  - Undulator
- Faults securely bypassable with user authentication

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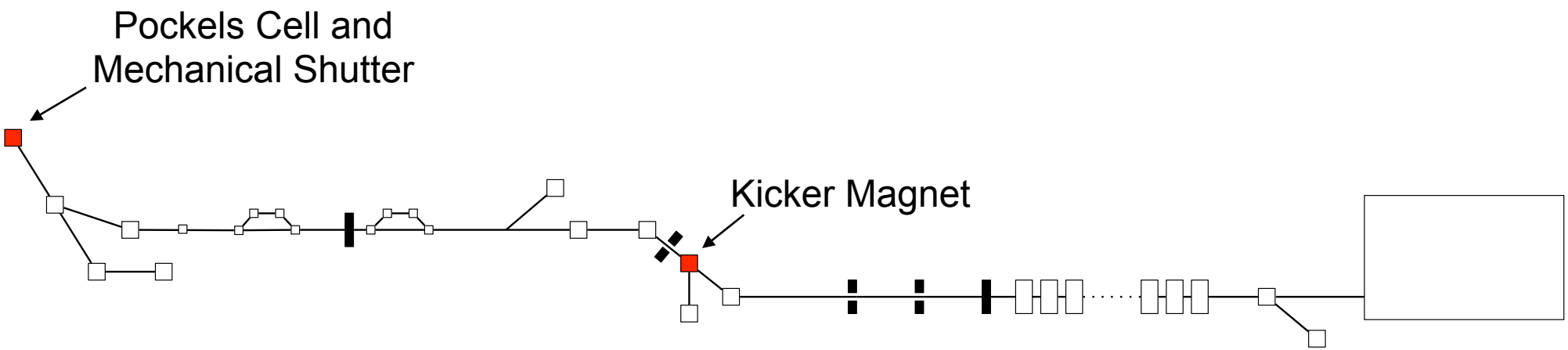
Beamline Schematic—Mitigation Devices



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Interim MPS

- Using old SLC protection system
- Updated and running successfully
- Interim MPS is sufficient for commissioning BC2
- New LCLS MPS will run in parallel to Interim MPS during BC2 commissioning
- After BC2 Commissioning
  - Timing requirements become more strict
  - New devices (beam loss monitors) are inputs to MPS
  - Protection of the machine can only be handled by the LCLS MPS

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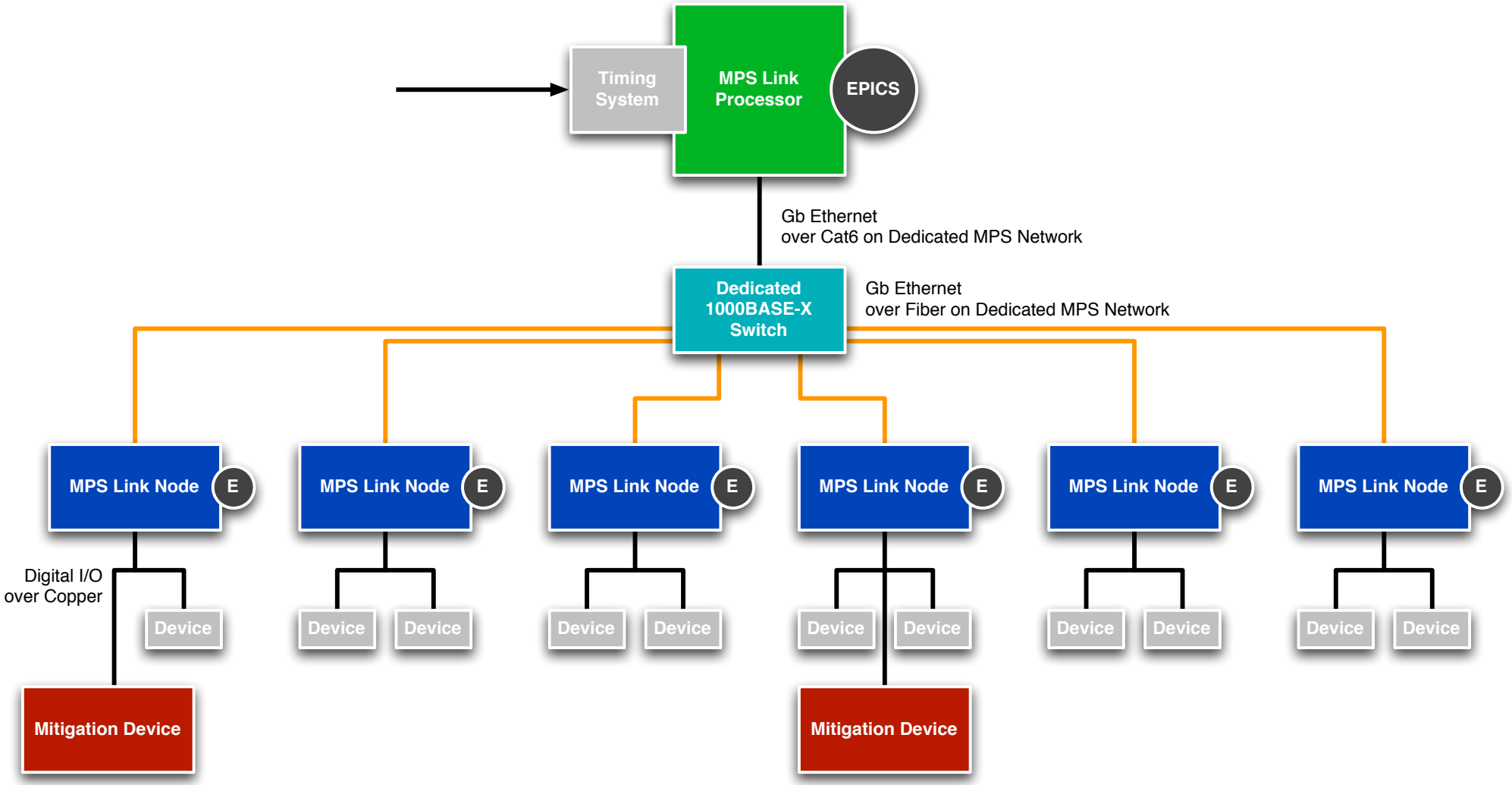
LCLS MPS Overview



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MPS Link Processor

- The brains of the MPS
- Gathers fault information from MPS Link Nodes
- Determines maximum allowable beam rate using this information
- Sends mitigation control signals out to MPS Link Nodes
- Interfaces with EPICS, timing system, MPS Link Nodes

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MPS Link Processor — Hardware

- Motorola MVME 6100
  - Machine protection logic
  - Interface to MPS Link Nodes (Gb Ethernet on Dedicated Network)
  - Interface to EPICS (Ethernet on Controls Network)
  - Synchronization of timing system and beam rate limiting
- Micro-Research Finland PMC-EVR-200
  - Interface to timing system
- Hardware is COTS and is used in other LCLS Projects

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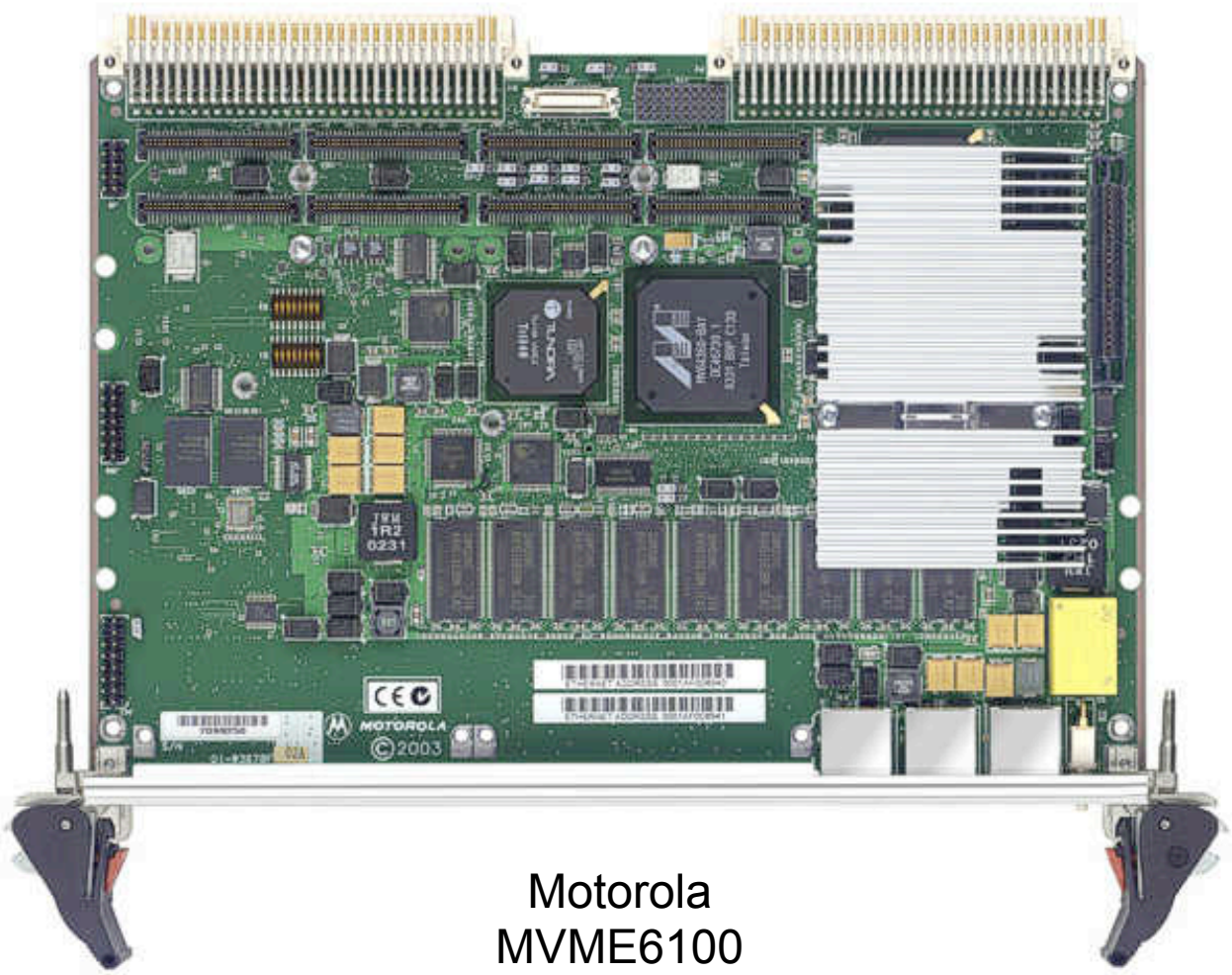
MPS Link Processor



Motorola
MVME6100

Micro-Research
PMC-EVR-200

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MPS Link Node

- Xilinx Virtex-4 FX20 FPGA
  - Interface to digital input and output cards
  - Communication with MPS Link Processor over Gb Ethernet
  - Does not rely on ColdFire for fault communication
- Arcturus ColdFire Processor
  - SLAC supported RTEMS/EPICS
  - Remote diagnostics and configuration of FPGA only
  - Reports detailed fault information to users
- Digital Input and Output Cards
  - Inputs for device faults and status
  - Outputs for device control

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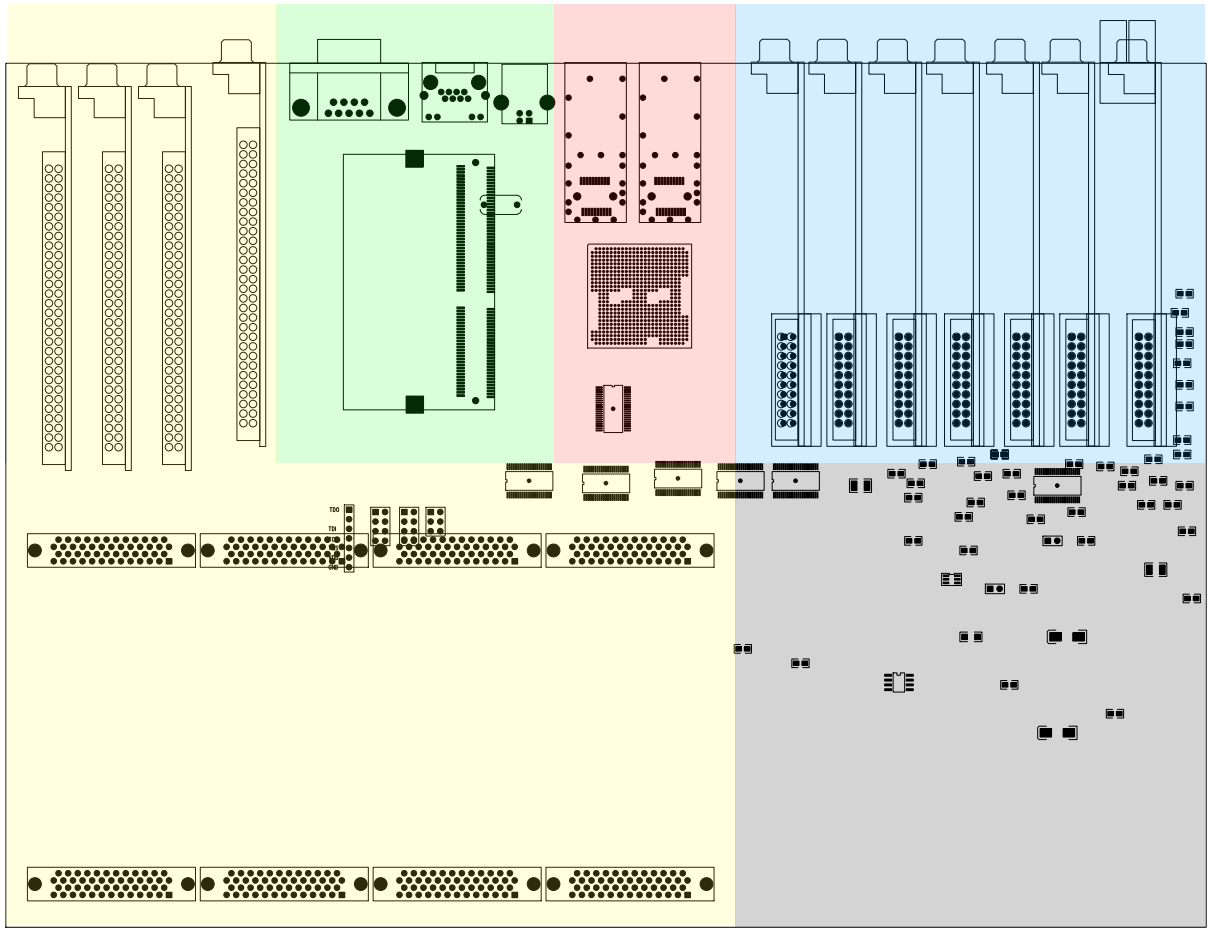
MPS Link Node — Circuit Board Layout



Arcturus ColdFire

FPGA and Fiber TxRx

Configurable Digital I/O

Expandability

Board Support

- Gb Ethernet over fiber
- Configurable I/O
- Up to 96 Inputs
- Processor running RTEMS/EPICS
- SLAC designed

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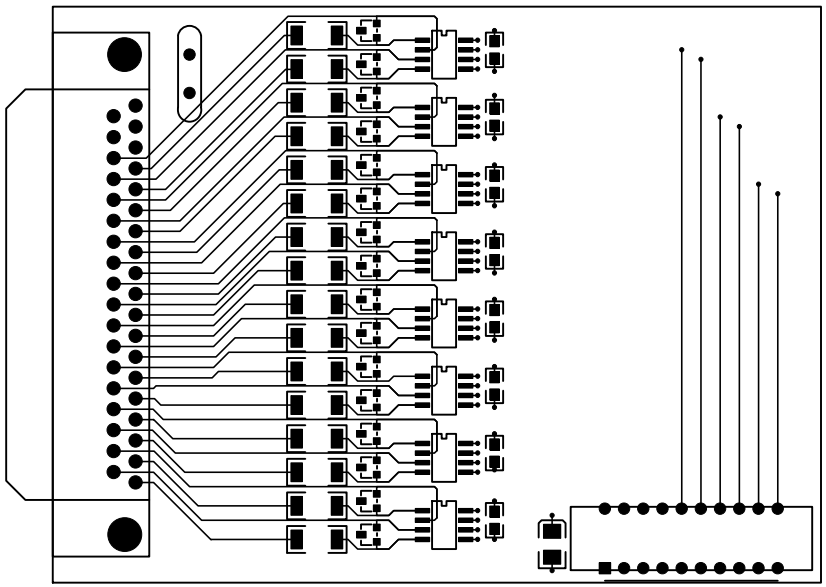
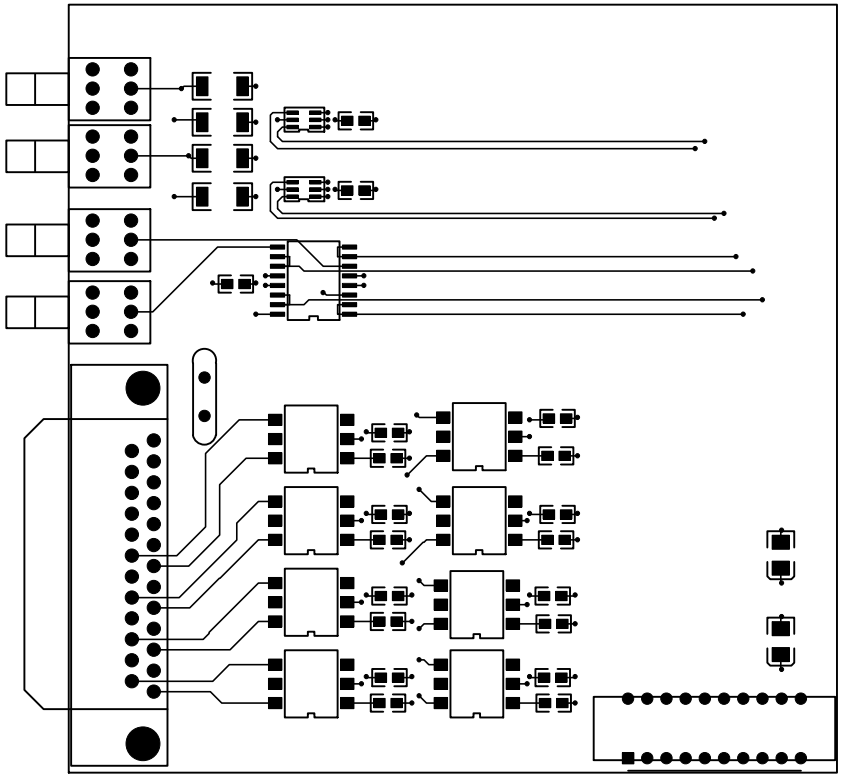
MPS Link Node I/O



Input Card



Output Card

(SLAC designed)

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MPS Fault Devices

- Limit Switches
  - Vacuum Valves
  - OTRs
  - YAGs
  - Mirrors
  - Stoppers
- Magnet Status
- Flow Switches
- Analog Level Threshold Exceeded
  - Joule Meter
  - Protection Ion Chambers
  - PLIC
  - Toroids
- Mitigation Devices

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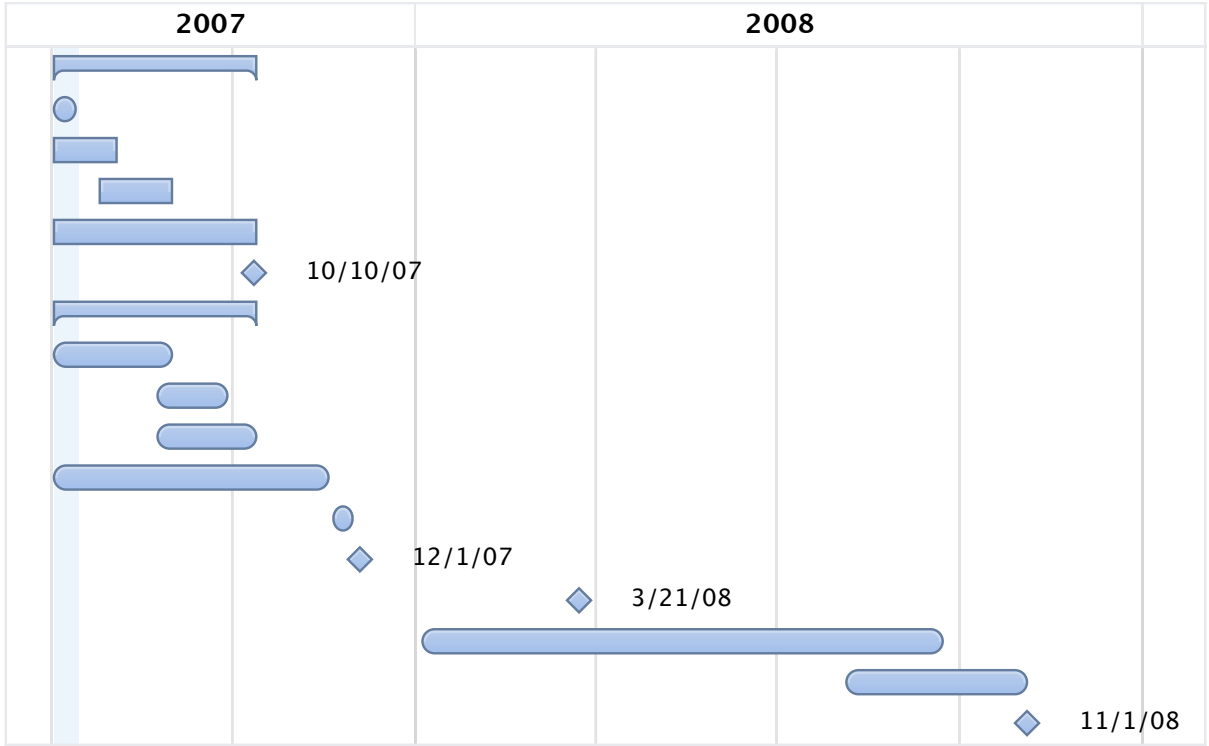
Schedule

Task	End
1) MPS Link Processor	**10/10/07**
1.1) Communication Protocol	7/11/07
1.2) Gb Ethernet	8/1/07
1.3) Timing Integration	8/29/07
1.4) MPS Link Processor Software	10/10/07
2) PDR	10/10/07
3) MPS Link Node	**10/10/07**
3.1) Hardware Fabrication	8/29/07
3.2) FPGA Firmware	9/26/07
3.3) ColdFire Software	10/10/07
4) User Interface	11/15/07
5) Partial Installation	11/28/07
6) System Testing (BC2 Commissioning)	12/1/07
7) FDR	3/21/08
8) System Testing	9/19/08
9) Interlock Hardware Testing	10/31/08
10) Undulator Commissioning	11/1/08



Task Assignment

Task/Position	Assignment
1) Project Lead	P. Krejcik
2) Technical Lead	S. Norum
3) User Interface	D. Murray, A. Alarcon
4) Interlock Hardware Testing	A. Tilghman
5) MPS Link Processor Software	S. Norum
a) Communication Protocol	T. Straumann
b) Gb Ethernet	T. Straumann
c) Timing Integration	S. Allison
6) MPS Link Node Hardware	J. Olsen
7) MPS Link Node FPGA	J. Olsen, S. Norum
8) MPS Link Node PPC	D. Kotturi
9) EVG Software	S. Allison

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