Total Energy Monitor Electronics

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8/12/08

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8/4/08

Summary: This document analyzes and summarizes the electronics for the Total Energy Monitor (TE) system.

Change History Log

<table>
<thead>
<tr>
<th>Rev Number</th>
<th>Revision Date</th>
<th>Sections Affected</th>
<th>Description of Change</th>
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<tr>
<td>000</td>
<td>2008/7/31</td>
<td>All</td>
<td>Initial Version</td>
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Auspices Statements
This work was performed under the auspices of the U.S. Department of Energy by University of California, Lawrence Livermore National Laboratory under Contract W-7405-Eng-48. Work supported in part by the DOE Contract DE-AC02-76SF00515. This work was performed in support of the LCLS project at SLAC.
Article I. TEM Overview.................................................................4
Section 1.01 Block Diagram..........................................................4
Section 1.02 Requirements............................................................5
Section 1.03 Key Delivery Dates....................................................6

Article II. Theory of operation:...................................................7
Section 2.01 Overview ................................................................7
Section 2.02 Lab Measurements ..................................................7
(a) Lab Setup and Material Overview ...........................................7

Article III. Pre-Amp Detailed Design ...........................................8
Section 3.01 Overview ................................................................8
Section 3.02 Amplifier Stage .........................................................8
(a) Bias Bridge and input range ..................................................8
(b) System Gain ........................................................................11
(c) Noise EMI suppression and limiting spurious oscillations .......13
(d) Pre-Amp Response .............................................................13
(e) Noise Calculation ...............................................................15
Section 3.03 Precision and repeatability of measurement ..........18
Section 3.04 Regulator .................................................................20
(a) Overview ............................................................................20
(b) -5V regulator Operation Theory .........................................21
(c) Thermal .............................................................................22
(d) +5V regulator .................................................................23

Article IV. Grounding, Shielding and Noise environment ..........23
Section 4.01 Shielding .................................................................23
Section 4.02 Ground Loops ........................................................23
Section 4.03 Increasing Power Supply Rejection Ratio ..............24

Article V. Supporting Circuitry ....................................................27
Section 5.01 Bias Voltage .............................................................27
(a) Overview ..........................................................................27
(b) Circuit .............................................................................27
(c) Load Current .....................................................................27
(d) Single-Ended Supply Vs Differential Supply Bias ...............27
Section 5.02 Voltage Monitor .......................................................28
(a) Overview ..........................................................................28
(b) Calculations ....................................................................28
(c) Circuit .............................................................................28
Section 5.03 Energy Calculation ..................................................29
Section 5.04 Other ......................................................................30
(a) Cabling ............................................................................30
(b) Input protection using Diode clamps .................................31
Section 5.05 Layout Guidelines ..................................................31
(a) Rough Layout and Size Estimate .......................................31
(b) Choice of Layout House ....................................................32
Section 5.06 Testing .................................................................32
(a) Overview ..........................................................................32
(b) Off-line calibration capability to qualify circuit .................33
Section 5.07 Issues and Needs ...................................................34

Article VI. Pre-Amp Schematic ...................................................35

Article VII. BOM...........................................................................43
Article I. TEM Overview

Section 1.01 Block Diagram

Total Energy Electronics Overview
- 16 pre-amplifier sensor channels on one board
  - Each pre-amp has a gain 35.2V/V (30.9dB)
  - Energy Measurement error due to electronics is much less than the system requirement of ± 10% at 10 mJ and within ± 25% at 10 uJ.
  - Setup for the following input voltages (Vbias=+/−2V):
    - @1uJ Vin = 107uV
    - @10mJ Vin = 846 mV
  - Noise Performance:
    - @ lowest required input of 1uJ: SNR = 192 (0.5% error, 45.6dB)
    - @ highest required input of 10mJ: SNR = 1.8 x 10^5 (105dB)
  - Pre-Amp size: 8” by 11” including metal case.
  - If 32 sensors are required, another pre-amp board can be used in parallel.
    - No voltage monitoring will be possible in this configuration.
- 16 CMR input voltage monitors, one per sensor.
- Plan to cable 50 lines to the sensor head which will support 16 channels
  - Each sensor requires three lines: a Bias voltage input, CMR output, and Bridge output.
  - Two spare lines connected to ground.
• Bias Voltage and amplifier supply voltage are regulated voltages. The regulator voltages are derived from the power supplied by a spare VME board.
• ICS-121 : 32 channel signal conditioning board
  ➢ The Pre-amp is cabled to the ICS-121 using a 78 pin sub-D connector.
  ➢ Voltage gain of 0.25 V/V to 125 V/V (-12dB to 42dB) in 6dB steps
  ➢ Input filter of 100 KHz, the thermal signal response of the sensor is about 100usec.
• ICS-130 : 32 channel ADC.
  ➢ 16-bit
  ➢ SNR 80dB
  ➢ 1.2Mhz sampling, allows averaging/reduction of measurement noise.
  ➢ 2MSample buffer, collection is triggered by the start pulse of the FEL.
• VME interface

Section 1.02 Requirements

From PDR

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<th>Requirement</th>
<th>Section</th>
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<tr>
<td>1</td>
<td>No</td>
<td>Radiation hardness for FEL pulses from 0.8 to 8 keV required</td>
<td>NA</td>
</tr>
<tr>
<td>2</td>
<td>Yes</td>
<td>Dynamic Range: Operation from 1µJ/pulse to maximum FEL power of 2 mJ/200fs pulse required. Calculations suggest beam may be 2-3 times larger than ideal case. Pre-amp will accept 10mJ of input power</td>
<td>3.02.a, 3.02.b</td>
</tr>
<tr>
<td>3</td>
<td>Yes</td>
<td>Repeatability: &lt;1% at 0.2 mJ, and at full power. Sensor needs to handle beam jitter up to ±100 µm at 800 eV</td>
<td>3.02, 3.02.e, 3.03, 3.04.d</td>
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<tr>
<td>4</td>
<td>Yes</td>
<td>Rate of operation: 10 Hz required, 120 Hz desirable at full power</td>
<td>1.01</td>
</tr>
<tr>
<td>5</td>
<td>Yes</td>
<td>Absolute accuracy &lt;10% at 0.2 mJ</td>
<td>3.02.c</td>
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<tr>
<td>6</td>
<td>No</td>
<td>Range of validity specified (separation of FEL and spontaneous signal)</td>
<td>NA</td>
</tr>
<tr>
<td>7</td>
<td>No</td>
<td>Instantaneous field of view 3 × 3 mm²</td>
<td>NA</td>
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<tr>
<td>8</td>
<td>No</td>
<td>Field of regard ±5 mm horizontal and vertical</td>
<td>NA</td>
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Derived Requirements

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<th>Requirement</th>
<th>Section</th>
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<tbody>
<tr>
<td>9</td>
<td>X</td>
<td>Slow thermal signal over 300 micro seconds permits analog circuitry to have small bandwidth &lt; 100 kHz</td>
<td>3.02.d</td>
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<tr>
<td>10</td>
<td>X</td>
<td>Testability and calibration: Need to be able to test each channel independent of the sensor</td>
<td>5.03</td>
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<tr>
<td>11</td>
<td>X</td>
<td>Need to calibrate voltage-output-to-input-energy</td>
<td>5.02</td>
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<tr>
<td>12</td>
<td>X</td>
<td>Sample at high speeds, 1.2 M samples second (16bit), to allow averaging of output, to give consistent and precise measurement of pulse energy</td>
<td>1.01</td>
</tr>
<tr>
<td>13</td>
<td>X</td>
<td>Maximum output should utilize full ADC range of +/-5V</td>
<td>3.02.b</td>
</tr>
<tr>
<td>14</td>
<td>X</td>
<td>Should be supplied off +/- 7.5V from external source</td>
<td>3.04</td>
</tr>
<tr>
<td>15</td>
<td>X</td>
<td>Nominally run at ambient temperature, but should design for 40C.</td>
<td>3.04.c</td>
</tr>
<tr>
<td>16</td>
<td>X</td>
<td>CMR sensor material will change resistance according to its temperature coefficient of resistance, nominally 4.5Kohms/mJ. A bias voltage needs to be applied to measure this change of resistance.</td>
<td>5.01</td>
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<tr>
<td>17</td>
<td>X</td>
<td>Total Energy must be computed for each FEL pulse</td>
<td>5.02.b, 5.03</td>
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<tr>
<td>18</td>
<td>X</td>
<td>Design should be able to fit onto Total Energy Laser table.</td>
<td>5.05</td>
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Section 1.03 Key Delivery Dates

<table>
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<th>Date</th>
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<tr>
<td>2008-8-15</td>
<td>Final Design Review for Electrical Design</td>
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<tr>
<td>2008-8-25</td>
<td>To Layout and Fabrication</td>
</tr>
<tr>
<td>2008-10-1</td>
<td>Assembled board, begin testing and debug</td>
</tr>
<tr>
<td>2008-11-15</td>
<td>Finish Testing</td>
</tr>
<tr>
<td>2008-12-1</td>
<td>Lab measurement and write-up</td>
</tr>
<tr>
<td>2009-1-20</td>
<td>SLAC setup</td>
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<tr>
<td>2009-2-28</td>
<td>Hand off to SLAC</td>
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Article II. Theory of operation:

Section 2.01 Overview
The total energy system indirectly measures the energy of an FEL pulse. The FEL pulse duration is approximately 100 femto seconds. The FEL pulse will heat up the CMR material, which will change its resistance. By monitoring this change of resistance, the energy of the FEL pulse can be calculated.

Section 2.02 Lab Measurements
(a) Lab Setup and Material Overview
Initial lab tests were done to measure the CMR change of resistance and to determine the linearity of the system. The graph below shows the output voltage of the test circuit over the energy range of the test laser. Also shown is the calculated energy based on the output voltage and a comparison to the theoretical value.
Article III.  Pre-Amp Detailed Design

Section 3.01  Overview

Section 3.02  Amplifier Stage

(a) Bias Bridge and input range
The FEL pulse will heat the CMR material. The heated CMR material changes its resistance according to the value of the temperature coefficient of resistance (TCR). The strength of the FEL pulse is found by measuring the change in resistance. To measure this change of resistance, a bias voltage is placed across the material.

From the lab measurements, the change in temperature is \( \sim 1 \text{mJ/K} \). This change of temperature is proportional to a change in resistance per energy which is 4.5Kohms/mJ, or in terms of TCR, a change of 14%. The minimum pulse energy of 1uJ corresponds to a change in resistance of 4.5ohms. Likewise, the maximum pulse energy will be 10mJ which will give 45 Kohms.

Ideally, one would want a large current flowing through the material, in order to get a large change in voltage for a small change in resistance. The main issue with increased bias voltage is that the 1/f noise also increases with bias voltage.

Ideally, the bias voltage needs to impress a two volt drop across the CMR material, to limit the impact of the 1/f noise. The integrated noise across the input bandwidth is 17uV.
A differential bridge is used in conjunction with an op-amp, to limit the common mode noise. The differential bridge will have two equally-matched reference points to the input of the differential op-amp. Having a balanced input allows the noise that is introduced to appear equally on both sides of the bridge. Such common mode signals will be cancelled out in the amplifier. The CMRR of the AD8132 differential amplifier is -75dB.

The bridge configuration and equivalent input resistance to the op-amp is illustrated below:

By using this initial, unity-gain buffer configuration, the subsequent gain stage is decoupled from the input. This two-stage approach results in a gain that is independent of the bias bridge network and, equally important, allows the overall noise of the amplifier design to be reduced. This statement is not inherently obvious, but if one goes through the noise calculation for a one stage gain amplifier, the noise is proportional to the feedback resistor $R_f$ and effective gain resistor. The effective gain resistance is the combination of the bias bridge resistors and gain resistor of the amplifier. To get a large gain from one amplifier stage takes a large feedback resistor (10x larger than the two stage approach), which directly relates to a decrease in noise performance.

The input voltage to the amplifier as a function of the input pulse energy is calculated as follows:

\[
RG_{1_{eff}} := 2\cdot RG_1 + \frac{(R_{cmr}\cdot R_{ref})}{(R_{cmr} + R_{ref})}
\]

\[
RP_1 := \frac{R_{ref}\cdot RG_{1_{eff}}}{(R_{ref} + RG_{1_{eff}})} \quad \text{and} \quad \frac{R_{cmr} + R_{delta} + RG_{1_{eff}}}{R_{cmr} + R_{delta} + RG_{1_{eff}}}
\]

\[
Vin := \frac{V_{bias}}{2} \cdot \left[ \frac{RP_1}{(R_{cmr} + R_{delta} + RP_1)} \right] - \left[ \frac{RP_2}{(RP_2 + R_{ref})} \right]
\]

Looking at the minimum and maximum energy inputs, for a bias voltage of 4V, we get the following input voltage relation:

Vin(E_{min}) = 54.8uV
Vin(E_{max}) = 342 mV
A noise calculation shows that the noise voltage of the two-stage amplifier with this
direct signal feed will be 32.4uV, or SNR of 110 at the low energy input. This SNR
results in an error of ~1 % at low energy. Though this meets the requirement, this input
range is half of the possible theoretical performance of a resistive bridge. Environmental
factors such as the 1/f noise of the CMR material, single ended-noise, and part
tolerances will further limit the measurement, so having a larger dynamic range will give
us better performance. On another note, if the input op-amp is decoupled as much as
possible, then backing-out the energy input will become an easier calculation.

If the input bias resistor is decoupled from the input resistance using an emitter follower
configuration, then the dynamic range of the input will increase. This also allows the
gain of the amplifier to be turned down, which will decrease the noise component. The
emitter-follower configuration is as follows:

```
RCMR_Ref
33.8k
CMR
33.8k

Vbias/2
5V

+     -
U4
AD8138/AD
OUT+ 4
+8  -1
V+  3
V-  6
OUT- 5
VOCM2
Rre f
76k
Rre f
76k

RG1
510
RG1
510

RF1
510
RF1
510

-Vbias/2
-Vbias/2

To Next Stage
R27
10k
R27
10k

Q7
BC846_1
-R28
10k
-R28
10k

Q8
BC846_1

5V

RF1
510
RF1
510

To Next Stage
```

The reference resistor is adjusted to account for the base-to-emitter voltage drop, such
that the input voltage to the op-amp will be centered at zero volts. From the Vin
equation above, the parallel resistances of RP1 and RP2 are dependent more on the
reference resistance instead of the gain resistor, as the bridge now sees an input
resistance of hfe*RG1. Assuming hfe = 100, the effective input resistance is 51kohms.
The new input signal voltages are as follows:

\[
\begin{align*}
\text{Vin}(\text{Emin}) &= 107 \text{ uV} \\
\text{Vin}(\text{Emax}) &= 846 \text{ mV}
\end{align*}
\]

The transistors are selected to be equally matched as well as having a low noise
component. The noise component of the transistor is 123 nV. The transistor changes
the noise component of the first stage, but only by a small margin (<40nV). The SNR
for the minimum input is now calculated to be 192 V/V, or an error of 0.5% of the
desired signal.

The following figure shows the input signal range for implementation with and without
the emitter-follower configuration.
(b) System Gain

The system gain of the pre-amp is defined by the first and second stage. The following statements will go through the calculations of the system gain.

The first stage gain is proportional to the feedback resistor over the input gain resistor. The input gain resistor is the combination of $RG$ and the output impedance of the emitter follower. The combined output impedance of the emitter follower is the load resistor parallel to the transistors internal impedance $Z_{out}$. Due to the transconductance value of the transistor, the dominating term is $\frac{(R_{cmr}|R_{pref})}{hfe}$ and the load resistor can be ignored in determining the effective resistance. The effective source impedances $Rs$ and $Rb$ are defined as follows:

$$Rs := \frac{R_{cmr}R_{ref}}{hfe\cdot(R_{cmr} + R_{ref})}$$

$$Rb := \frac{R_{cmr}\cdot b\cdot R_{ref\cdot b}}{hfe\cdot(R_{cmr\cdot b} + R_{ref\cdot b})}$$

The gain of the first stage of the differential amplifier is defined as:

$$Gain_{1b} := 1 + \left[\frac{RFn}{(Rb + RGp)}\right]$$

$$Gain_{1s} := 1 + \left[\frac{RFp}{(Rs + RGs)}\right]$$

$$Gain_{S1} := Gain_{1s} + Gain_{1b}$$

The Gain of the first stage is equal to 3.52V/V.
The second stage of the pre-amp is shown in the scaled-down schematic below. The gain is proportional to the gain resistor RG2 and feedback resistor RF2. Note that the output impedance of the first stage is very small, so it can be ignored in determining the gain of the second stage.

\[
\text{Gain}_{2s} := \frac{RF_{2n}}{RG_{1n}} \quad \text{Gain}_{2b} := \frac{RF_{2p}}{RG_{1p}}
\]

\[
\text{Gain}_{S2} := (\text{Gain}_{2s} + \text{Gain}_{2b})
\]

The static gain of the second stage is equal to 22.0 V/V.

\[
\text{Gain}_{S1S2} := \text{Gain}_{1s}\text{Gain}_{2s} + \text{Gain}_{1b}\text{Gain}_{2b}
\]

The total gain is equal to 35.2 V/V

The theoretical Differential Vout @ the minimum and maximum energy inputs:

\[
\text{Vout (1uJ)} = 3.8 \text{ mV}
\]

\[
\text{Vout (2mJ)} = 8.8 \text{ V}
\]
(c) Noise EMI suppression and limiting spurious oscillations
An input Low Pass Filter is used on the input to improve signal measurements, by reducing the total input bandwidth and increasing the CMRR.

Bypass capacitors are used on all operational amps to reduce noise on the power supplies and to suppress oscillations from occurring within the op-amps.

(d) Pre-Amp Response
Using a Pspice simulator, the pre-amp was run over varying energy inputs to look at the transient response, AC response, and CMRR of the design. The following Pspice analysis are highlights of the pre-amp performance.

Transient Minimum Energy Input Response: The following figure shows the Pre-amp response to the minimum energy input pulse of 143uV. The minimum input is shown in red, with a pulse length of 1ms. Shown on the upper plot is channel one of the pre-amp output with a 1.43mV peak to peak signal.
Transient Maximum Energy Input Response: The following figure shows the Pre-amp response to the maximum energy input pulse of 220mV. The input is shown in red, with a pulse length of 1ms. Shown on the upper plot is channel one of the pre-amp output with a 2.2V peak to peak signal.

AC Response with Input Filter:
The top plot on the following figure shows that the AC response is linear over the bandwidth of concern.
Common-Mode Rejection:
The following frequency analysis shows that the pre-amp has over 100dB of common mode rejection over the bandwidth of interest.

(e) Noise Calculation

The requirements specify ±10% maximum error at an energy input of 200uJ. The total error of the system includes, but is not limited to, the noise of the electronics, sensor impurities, and FEL pulse scattering. Since the electronics is only a fraction of the system error, the error due to the electronics should be much less than the 10% requirement.

Each component of the Pre-Amp circuit will contribute to the total noise in the system. The noise of each stage will be the sum of each noise component squared. Resistors have thermal noise which is integrated over the input bandwidth. The signal bandwidth is from 10Hz to 100KHz. The Op-amp will have both voltage and current noise as a function of thermal noise and 1/f noise integrated over the Input Bandwidth.

The noise introduced by the sensor, reference and bridge resistor is as follows:

\[
N_s := \left[4 - \frac{2}{\text{BW}} \left( \frac{(\text{Rcmr} - \text{Rcmr}) \cdot \text{TRcmr}}{(\text{Rcmr} + \text{Rcmr}) \cdot \text{TRcmr}} \right) \right]^{1/2} \\
N_b := \left[4 - \frac{2}{\text{BW}} \left( \frac{(\text{Rcmr} \cdot \text{Rcmr} + \text{TRcmr}) \cdot \text{TRcmr}}{(\text{Rcmr} \cdot \text{Rcmr} + \text{TRcmr}) \cdot \text{TRcmr}} \right) \right]^{1/2}
\]
Where

- BK is Bulkmans Constant of 1.38E-23
- BW is the input Bandwidth: 100KHz-10Hz
- TRcmr is the temperature of the CMR material: 100K
- TRref is the ambient temperature of the pre-amp: 300K

The noise due to the reference bridge was calculated to be:

\[ \begin{align*}
Ns &= 1.15 \mu V \\
Nb &= 1.15 \mu V
\end{align*} \]

The AD8132 has a noise specification of 9.6nV/Hz^{1/2} at 100KHz. This is the white noise component. The AD8132 also specifies 2uV/Hz^{1/2} at 10Hz. This used to calculate the 1/f noise:

\[ N_{eff}(f) := N_0 + A_e f^{E_e} \]

The noise voltage is then integrated over the bandwidth, as shown in the following equation:

\[ Net := \left( \int_{f_1}^{f_2} N_{eff}(f) \frac{df}{2} \right)^{1/2} \]

The noise voltage of the op-amp is calculated to be:

\[ Net = 2.61 \mu V \]

Likewise the noise due to the current source is computed as:

\[ N_{it}(f) := N_{io} + A_i f^{E_i} \]

\[ N_{it} := \left( \int_{f_1}^{f_2} N_{it}(f) \frac{df}{2} \right)^{1/2} \]

The current noise of the op-amp is calculated to be:

\[ N_{it} = 68.9 \text{nV} \]

The total noise due to stage one is:

\[ N_{stage1} := \left[ N_s^2 \left( \frac{RF1_n}{R_s} \right) + N_b^2 \left( \frac{RF1_p}{R_b} \right) + N_{it}^2 \cdot RF1_p + N_{it}^2 \cdot RF1_n + Net^2 \left( \frac{RF1_n}{R_s} \right) + Net^2 \left( \frac{RF1_p}{R_b} \right) \right]^{1/2} \]
RF1, Rs, and Rb are the values specified in the gain calculations. Ns and Nr are the noise due to the reference bridge. Nit and Net are the current and voltage noise due to the op-amp. The resulting noise due to stage one is:

\[ N_{\text{stage1}} = 7.198\mu V. \]

A quick look at the noise from the emitter-follower is as follows:

Where the Nemitt over the input bandwidth is 135 nV and the noise in stage one is now:

\[ N_{\text{stage1}} = \left[ N_{\text{stage1}}^2 + \text{Nemitt}^2 \left( \frac{RF1n}{Rs} \right) \right]^{\frac{1}{2}}. \]

The newly-calculated noise is:

\[ N_{\text{stage1}} = 7.202\mu V \]

Which is a difference of 4nV vs no emitter follower.

Using the same method, the noise of the second stage can be calculated:

\[ N_{\text{stage1b}} := \left[ Nb^2 \frac{RF1p}{Rb} + Nit^2 \cdot RF1p + Net^2 \left( RF1p \right) \right]^{\frac{1}{2}}. \]

\[ N_{\text{stage1s}} := \left[ Ns^2 \frac{RF1n}{Rs} + Nit^2 \cdot RF1n + Net^2 \left( RF1n \right) \right]^{\frac{1}{2}}. \]

\[ N_{\text{stage2}} := \left[ N_{\text{stage1s}}^2 \left( \frac{RF2p}{RG1p} \right) + N_{\text{stage1b}}^2 \left( \frac{RF2p}{RG1p} \right) + Nit^2 \cdot RF2n + Nit^2 \cdot RF2p + Net^2 \left( \frac{RF2n}{RG1n} \right) + Net^2 \left( \frac{RF2p}{RG1p} \right) \right]^{\frac{1}{2}}. \]

The resulting noise for stage two and the pre-amp is calculated to be:

\[ N_{\text{stage2}} = 32.4\mu V \]

Looking at the Signal-to-Noise Ratio (SNR) will show that the error created by the noise in the system is:

\[ \text{SNR} := \frac{V_{\text{sig}} \cdot \text{GainS1S2}}{N_{\text{stage2}}}. \]

Where the gain is 56V/V and Vsig is the input signal created by the change in voltage across the Sensor. The SNR for the minimum input is now calculated to be 186 V/V, or
an error of less than 1% of the desired signal. At the maximum signal input, the SNR is 11.4 KV/V. The following is a plot of SNR for theoretical performance vs. the required SNR as a function of energy input.

![SNR plot](image)

**Section 3.03 Precision and repeatability of measurement**

The error from the electronics is due to the noise of the components, component tolerances, and part drift.

The precision error is defined as:

\[
\text{Precision\_Error} = \text{Error\_Noise} + \text{Error\_Drift} + \text{Error\_PartTolerance}
\]

Repeatability only includes the noise and drift components:

\[
\text{Repeatability\_Error} = \text{Error\_Noise} + \text{Error\_Drift}
\]

The tolerance in the output voltage is related to the precision of the gain value, Bias Voltage tolerance, and bridge tolerance.

The error on the gain is a function of the error on the feedback and gain resistors:

\[
\text{Err} = \frac{2}{\text{GainS1S2\_nom}} \left[ \frac{\text{RF2p(1 + tolerance)}}{\text{RG2p(1 – tolerance)}} \right] \left[ 1 + \frac{\text{RF1p(1 + tolerance)}}{\text{RG1p(1 – tolerance)}} \right]
\]

\[
\text{Err} := 100(1 – \text{Err})
\]

The resulting calculations at different tolerances are:

- @ 1% tolerance \(\text{Err(GainStage)} = 3\%\)
- @0.1% tolerance \(\text{Err(GainStage)} = 0.3\%\)

The error on the input voltage is related to the values in the bridge network. Note that the following calculation assumes that the CMR tolerance is the same as that of the selected resistors. This may not be a good assumption and will have to be monitored.
as the CMR sensors are fabricated, to ensure that the variance in CMR does not significantly affect the result.

The error due to the bridge is:

\[ \text{tolErr} = \frac{1 + \text{tolerance}}{1 - \text{tolerance}} \]

The resulting calculations at different tolerances are:

@ 1% tolerance  \( \text{Err(Bridge)} = 2\% \)
@ 0.1% tolerance  \( \text{Err(Bridge)} = 0.2\% \)

The last component is the bias voltage error. The value is computed in the bias voltage section:

@ 1% tolerance  \( \text{Err(VBias)} = 2.5\% \)
@ 0.1% tolerance  \( \text{Err(VBias)} = 0.25\% \)

The total part tolerance error is:

\[ \text{Error\_PartTolerance} = \text{Err(GainStage)} + \text{Err(Bridge)} + \text{Err(VBias)} \]

The resulting calculations at different tolerances are:

@ 1% tolerance  \( \text{Error\_PartTolerance} = 7.5\% \)
@ 0.1% tolerance  \( \text{Error\_PartTolerance} = 0.75\% \)

On the basis of part tolerances alone, the choice of 0.1%-tolerance parts is the correct choice. With that said, we also have the option of adding potentiometers to each channel, to effectively tune-out any error due to part tolerance.

By using low-tolerance parts, we also gain the advantage of a low TCR, 25ppm. By using a band-gap reference, the bias voltage will also have a low drift <0.002%. Using the same analysis above for drift, the error becomes:

\[ \text{Error\_Drift} = 0.005\% \]

The total system error, assuming 1%-tolerance parts and minimum energy input is:

\[ \text{Error\_Total} = \pm 1.3\% \]

The total system error for repeatability is determined at 0.2mJ. The noise component at 0.2mJ is 0.004%. So the repeatability error of the electronics is calculated to be:

\[ \text{Error\_Repeat} = \pm 0.009\% \]
Section 3.04 Regulator

(a) Overview
The amplifiers have a good power supply rejection ratio of \(-90\text{dB}\). The noise after rejection should be a factor of ten less than the output noise voltage at each stage. The noise after rejection should be less than 800nV. This translates to a noise value of 25mV on the regulator. Any nominal, linear regulator will work for this requirement.

On the other hand, the bias voltage is based off the band-gap reference. There is no power supply rejection in creating the bias voltage. So, care still must be used to keep the noise low on the 5 volt reference.

Using an input voltage of ±7.5volts will allow us to keep the power dissipation of the regulators at a minimum. Thermal considerations will still need to be followed, as stated in the analysis below.

Looking at the power requirements for 16 channels with the AD8132 amplifier, the current draw is 1.2 Amps. If the AD8138 is used, which has a better noise performance, the current draw is closer to 2.0 Amps. To allow flexibility in the design, the regulators must be able to supply a minimum of 3.0 Amps.

There are few high-amp, low-dropout (LDO), negative regulators to choose from, so an external MOSFET will be used to supply the extra current. Current-sense logic is used in conjunction with the MOSFET to allow proper current sharing and to maintain the protection that the regulator offers.
(b) -5V regulator Operation Theory

The regulator sets the output to a scaled factor of \( V_{\text{ref}} \), pin 1 on the regulator shown above. \( V_{\text{ref}} \) for the negative regulator is -1.25Volts.

\[
V_{\text{out}} = V_{\text{ref}} \times \left(1 + \frac{R_{44}}{R_{43}}\right)
\]

The op-amp modulates the on resistance of the n-channel MOSFET. This modulation forces the voltage drop across \( R_{42} \) to be the same as the drop across \( R_{50} \). With a ratio of ten-to-one in \( R_{42} \) to \( R_{50} \), the current through the MOSFET will be ten times greater than the regulator current. At the desired max current of 3A, the current through the MOSFET will be 2.7A and the current through the regulator will be 0.3A. The LM337 can supply 1.5A and the chosen MOSFET can supply 7.5A. Below is the pspice simulation output at these conditions:
(c) Thermal
All thermal considerations were calculated for a max ambient temperature of 50°C.

The regulator power draw is calculated as follows:

\[ P_{\text{reg}} = I_{\text{out}}(V_{\text{in}} - V_{\text{out}}) \]

Where \( V_{\text{in}} = 7.5\,\text{V} \) and, as stated in the theory of operation, the max current output of the regulator will be 0.3A, the power dissipated in the regulator will be:

\[ P_{\text{reg}} = 0.75\,\text{W} \]

The maximum rated junction temperature for the regulator must be below 125°C. The junction-to-ambient temperature is then defined as:

\[ T_{\text{ja}} < \frac{(T_{\text{jmax}} - T_{\text{a}})}{P_{\text{reg}}} \]

\[ T_{\text{ja}} < 100\,^\circ\text{C} /\text{W} \]

The SOT223 package can be used with a 1oz, square inch PCB mount, which will give a \( T_{\text{ja}} \) of 75°C/W.

The MOSFET power draw is calculated as follows:

\[ P_{\text{mos}} = I_{\text{out}}(V_{\text{in}} \cdot V_{\text{out}}) \]

Where, as above, \( V_{\text{in}} = 7.5\,\text{V} \) and the current required is 2.7A.

\[ P_{\text{mos}} = 6.8\,\text{W} \]

Using the same equation for the junction-to-ambient temperature, we find that:

\[ T_{\text{ja}} < 10\,^\circ\text{C} /\text{W} \]

This will require using the TO-252 package with a heat sink. This package and heat sink combination will give a \( T_{\text{ja}} \) of 3°C/W.
(d) +5V regulator
The analysis above also holds for the +5V regulator, except that a P channel MOSFET was used to supply the needed current in the design.

Article IV. Grounding, Shielding and Noise environment

Section 4.01 Shielding
Grounding will be done in accordance with IEEE recommendations. This will give the best grounding performance possible. Noise will be introduced into signal path as Common mode noise for the most part. The CMRR of the ICS Signal conditioning board is > 80dB.

The following picture shows how ground will be distributed in the system.

Section 4.02 Ground Loops
The main loop component is the ground noise coupled onto the Pre-Amp output. The following depicts the environment:

Estimating the ground noise requires consideration of:
- The noise generated by the backplane. The VME chassis purchased has a noise performance of < 15mVpp, typical <10mVpp (0-20MHz), 3mVrms (0-2MHz).
• Ground currents: The Ground wire has 0.012ohms/meter, over 5meters. Typical noisy environments have ground currents around 1Amp. Therefore the noise generated by ground currents will be about 60mV.

The rejected noise voltage must be less than 3.3uV, for the pre-amp minimum voltage output of 3.4mV, with a 1% error. The requirement will be at least 60dB of CMRR on the ICS board. The CMRR rejection of the ICS-121 is 80dB across the signal bandwidth. The actual noise voltage can be as high as 33mV.

Section 4.03 Increasing Power Supply Rejection Ratio

The design should filter out the worst-case noise from the power supply, to avoid degradation of system performance over the pulse energy input range.

The main components of power supply noise are:
• Reference voltage noise that comes from the VME power supply.
• Noise picked up in sending DC power from the VME crate to the pre-amp
• Power Regulator Noise: All regulators generate some noise that is added directly to the output.
• Signal Coupling onto the PC power: this is a mitigated by following proper layout techniques.

To help mitigate noise, the following will be done:
• VME power will be regulated on a VME breadboard that will reduce the VME noise to no more than 0.2Vpkpk ripple on either voltage rail going to the Pre-Amp.
• Power that is cabled to the Pre-Amp will be in a shielded twisted pair with a ground conductor.
• The Design Reviews suggested that filtering be done post-regulator. Due to the high current demands of the pre-amp, the filter must have a very high cut-off frequency. Several small resistors could be used going to each op-amp, but the likelihood of inductance-loop introduction, as stated in "Power Supply Ripple Rejection and Linear Regulators: What’s all the noise about?" (Planet Analog, http://www.planetanalog.com) is a possible consequence.
• Active filters in front of the LDO regulator were considered too much of a risk. As the risks include increased heat dissipation and/or an onboard oscillator which has the potential to propagate onto the signal path.
• A good compromise is to use a low-pass filter before the regulator. This allows the use an inductor with a small DC resistance and a small enough 3dB point to give the desired system performance. The rejection at 100KHz is -90dB for a passive filter compared to -100dB for the active filter. Note that there is little difference up to 100KHz.
• Capacitors on reference voltage will be used
• Bypass caps that will be placed near the input power connector.
• The output capacitor of the regulator is chosen to have a low equivalent-series-resistance value, less than 4 ohms.
• The use of differential amplifiers allows the noise from the regulator to be rejected as a common-mode component.
Largest voltage drop the system can permit is \(~0.3V\) on the +/-5V supply. With a 10uF cap and 0.1ohm resistor, the 3dB frequency is 159KHz. This 3dB point will improve out-of-band response, but will not have an effect within bandwidth. Using an NMOS/charge-pump filter in front of the LDO will improve in-band and the out-of-band response by a minimum of 20dB.

As mentioned in the article from Planet Analog, "Power Supply Ripple Rejection and Linear Regulators", adding filtering after a power supply can create inductance loops, so even though you added filtering to the out-of-band signal, you have opened the circuit up to loop problems.

The following graphs show the frequency response of the regulator and total noise response of the system. The rejection ratio can be greatly increased by adding filtering on the front of the LDO. Adding decoupling resistors between the LDO and the OP-amps was ruled out because only out-of-band performance is improved and there is an increased probability of introducing inductance loops within the design.
Article V. Supporting Circuitry

Section 5.01 Bias Voltage

(a) Overview
The bias voltage must be stable over time, such that it does not drift significantly over
time, and so affect the accuracy of the results. The bias regulator has low drift, 100ppm,
but has a tolerance of ±3%. So, even though the regulator satisfies the accuracy
requirement of 1%, it does not satisfy the precision requirement. This leads us to use a
bandgap reference that offers a low-drift component of 25ppm as well as a very
accurate reference of ±0.5%.

(b) Circuit

![Bias Voltage Circuit Diagram]

The LT1634 is a Zener IC bandgap voltage reference. It produces a stable 2.5V for the
input of the AD8132. The amplifier can be use in a single-ended configuration with a
gain that gives the required bias voltages.

(c) Load Current
Each bias bridge requires 320uA at a bias voltage of 2V. The AD8132 is rated to 95mA
on a 500ohm load. The design should stay at about half the rated maximum current
load for the AD8132. This would allow us to place about 10 channels per bias voltage
chain. The design will use four bias voltage generators, each supplying four channels.

(d) Single-Ended Supply Vs Differential Supply Bias
During initial integration with the FEL pulse, it may be decided that a better thermal
response in the CMR material can be produced using a single-ended supply vs a
differential supply, as shown above. To accommodate this change, the zero ohm

jumper can be removed and the bypass cap shorted to ground. This will allow either a negative or positive, single supply voltage bias for the CMR sensor.

**Section 5.02 Voltage Monitor**

(a) Overview

Knowing the steady-state input voltage will allow calculation of the CMR resistance. We can also use the monitor voltage to back-out the actual input reference voltage. This will allow us to pre-calibrate the system and will aid in determining the input-pulse-energy-to-change-in-output-voltage ratio.

(b) Calculations

The CMR resistance is calculated from the following equation:

\[ R_{cmr} = \frac{(V_{bias^+} - V_{monitor})}{I_{cmr}}. \]

Where \( I_{cmr} \) is defined as

\[ I_{cmr} = \frac{(V_{monitor} - V_{bias^-})}{R_{ref}} \]

For example, the monitor voltage is 761mV, \( V_{bias} = \pm 2V \) (known from the design) and \( R_{ref} = 76k \).

\[ I_{cmr} = \frac{(.761 + 2)}{76e3} = 36.5 \mu A \]

\[ R_{cmr} = \frac{2 - .761}{36.5\mu A} = 33.6 \text{ kohms} \]

The actual CMR resistance for this example is 33.3kohms. The error, which is less than 1%, is due to the non-ideal effective input resistance of the emitter-follower and amplifier combination. The error will also increase with variations in the bias voltage and the part tolerance of the reference resistor. This extra error will be under ½ percent. The complete error of the measurement will be about 1%.

(c) Circuit

The voltage monitor is a simple op-amp in a follower configuration. The follower configuration has very high input impedance when looked at from the bridge output. This high impedance is the ideal case, as it will not affect the dynamic range of the bridge. An extra op-amp is used to drive the differential lines to the ADC, to ensure that no extra noise is introduced into the measurement.

The op-amp chosen has much less current draw than the input amplifiers and will not add a larger power requirement for the regulators.
Section 5.03 Energy Calculation

- Will include C-code, as final deliverable, that calculates the pulse energy input based on the collected data from the 32 channel ADC VME board.
- Change E is equal/proportional to the change in output voltage of the pre-amp calculated as follows:

Example:

\[ V_{oss} := 0.1 \] Steady State output Voltage
\[ V_{monitor} := 0.7 \] Steady State Monitor Voltage
\[ V_{peak} := 1 \] Maximum Output Voltage

From Design:

\[ R_{ref} := 75 \times 10^3 \] Bridge Reference Resistor
\[ V_{bias_p} := 2 \] Positive Bridge Voltage
\[ V_{bias_n} := -V_{bias_p} \] Negative Bridge Voltage
\[ Gain_{S1S2} := 56.6 \] Pre Amp Gain
\[ Ch := 1 \times 10^{-3} \] Heat Capacitance 1mJ/K
\[ TCR := 0.14 \] Temp Coeffiecient of Resistance %/K

Steady State Calculations

\[ I_{cmr} := \frac{(V_{monitor} - V_{bias_n})}{R_{ref}} \] \[ I_{cmr} = 3.6 \times 10^{-5} \]
\[ R_{cmr} := \frac{(V_{bias_p} - V_{monitor})}{I_{cmr}} \] \[ R_{cmr} = 3.611 \times 10^4 \]
\[ Vin := V_{ref} - \frac{V_{peak}}{Gain_{S1S2}} \] \[ Vin = 0.681 \]


**Section 5.04 Other**

(a) Cabling

**From Sensor to Pre-Amp Cable Requirements:**

16 channels, where each channel has two signal lines and a bias voltage. 48 lines in total.

At minimum, each channel should have a twisted pair for each of the signal pairs. Ideally the signal pairs should be twisted with the corresponding bias voltage line. This may have to be a special-made cable or a cable that has four twisted lines where the fourth spare line is connected to ground.

- No smaller than 22 gauge wire.
- Needs to attach to 50pin sub-d connector on both the sensor and pre-amp.
- Needs to be slightly flexible to allow connection.

- Low Smoke
- NON-Halogen

**From Pre-Amp Cable to the ICS-121 Shaping board**

32 differential channels.

- Twisted pair for each channel.
- At minimum 5 meters of cable needed.
- No smaller than 22 gauge wire.
- Needs to attach to 78 pin sub-d connector on both the pre-amp and ICS board.
- Needs to be slightly flexible to allow connection.

- Low Smoke
- NON-Halogenated

---

FEL Energy Calculations

\[
\begin{align*}
V_{\text{ref}} &= V_{\text{monitor}} - \frac{V_{\text{oss}}}{\text{GainS1S2}} \quad \text{Vref = 0.698} \\
R_{\text{cmr.d}} &= R_{\text{ref}} \cdot \frac{(V_{\text{bias.p}} - V_{\text{in}})}{(V_{\text{in}} - V_{\text{bias.n}})} \quad \text{Rcmr.d = 3.692} \times 10^4 \\
R_{\text{delta}} &= R_{\text{cmr.d}} - R_{\text{cm}} \quad \text{Rdelta = 805.578} \\
E_{\text{delta}} &= \frac{(R_{\text{delta}} \cdot \text{Ch})}{R_{\text{cmr.TCR}}} \quad \text{Edelta = 1.593} \times 10^{-4} \\
\text{Energy in Micro Joules} &= E_{\text{uJ}} = 159.345
\end{align*}
\]
(b) Input protection using Diode clamps

Schottky diodes will clamp the input to the positive and negative supplies. Schottky diode clamps are also used on the output of the voltage regulator to prevent voltage spikes/shorts.

Section 5.05 Layout Guidelines

(a) Rough Layout and Size Estimate

- Board will be approximately 7" by 10"
- Channels 1-8 will be on top of the board and channels 9-16 will be on the bottom side.
- Board will be housed in shielded box.
(b) Choice of Layout House

Due to the low-noise requirements on the pre-amp, it is imperative that correct part placement and routing is followed. It is felt that by keeping the layout process in-house, we could easily monitor and make changes to the layout as it develops, as most of the noise problems are not apparent until the layout begins. Although inside work is 30% more costly than the outside design houses, the cost is made up in that the first iteration is much closer to what is needed to meet the requirements.

Section 5.06 Testing

(a) Overview

- Debug Board will allow independent testing of pre-amp, to be built-up on bread board.
- Use the same connector to be used on the feedthrough.
- Push button control to allow simple injection of signal at various pulse energy inputs.
- Dip switch used on each channel to selectively enable/disable test sensors.
- Decade Potentiometers set up to give wide range of simulated sensor input
- Analog switches allow for one button test of each channel
  - A small resistance is in the switch path, which is less than 4ohms.
  - Make-before-break switch
(b) Off-line calibration capability to qualify circuit

Final calibration will be made with the laser. This is done by monitoring the bias voltage of the bridge and backing-out the actual CMR resistance. Validation of the Pre-amp will be made with the Sensor Simulation board and VME crate.

Functional design testing with test board and oscilloscope:
- Voltage Monitoring and CMR resistance calculation
- Bias Voltage generation
- Power Supply and ripple
- Gain Performance
- Noise Performance
- Precision and reliability of Op-Amp output.

Test with VME board
- Test data collection, test drivers and gui operation.
- Verify Energy Calculations.
- Verify vs oscilloscope testing.

Laser Testing
- Final Calibration of system response over the energy range of 1uJ to 2mJ.
Section 5.07 Issues and Needs

- Issues:
  - Possible Noise caused by channel cross-talk through the bias voltage. This should be mitigated by using bias caps on all voltage rails.
  - Non-Linear Measurements with one stage sample pre-amp.
    - Diode affect is occurring with CMR material, which affects the change-of-resistance-for-input-pulse-energy curve.
    - More lab measurements and analysis of the data is required to give a better TCR ratio and overall translation between pulse energy and change of output voltage.
Article VI. Pre-Amp Schematic

(i) PG1
(iii) PG3

(iv) PG4
(v) PG5

(vi) PG6
(xi) PG11

(xii) PG12
(xiii) PG13
## Article VII. BOM

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