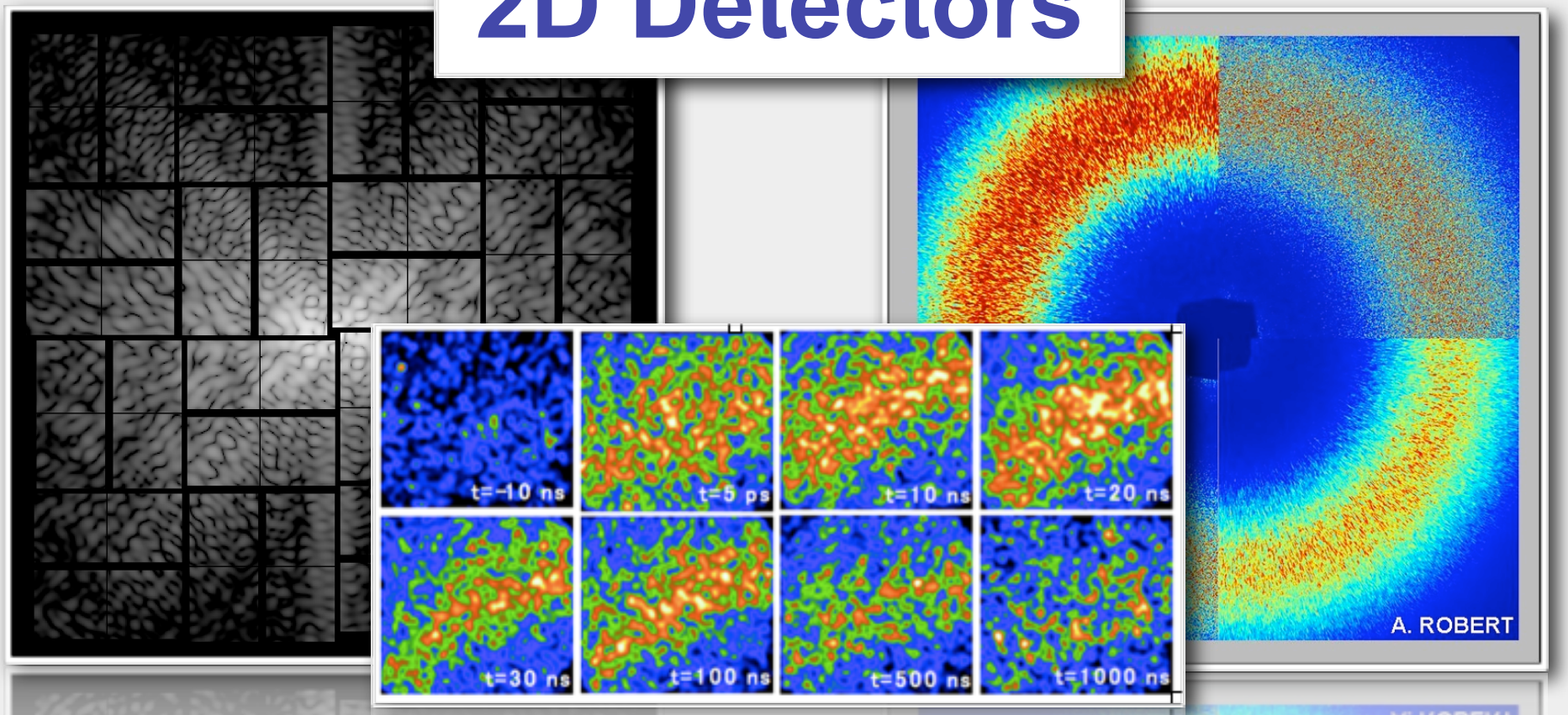
2D Detectors



Niels van Bakel – Detector Physicist

April 21, 2009

Outline

- Detector program
- XPP detector
  - Requirements & Technical progress
- XCS detector
  - Requirements & Technical progress
- CXI detector
  - Requirements & Technical progress
- Interfaces; mechanical & DAQ
- Summary & Outlook

BNL Team

- Detector Development Group to bring advanced detectors to NSLS users for several years
  - Primary expertise is embedded computing, system integration and x-ray science
    - Peter Siddons; project leader
    - Kate Feng, Tony Kuczewski, Rich Michta, Joe Mead; DAQ and user interface
    - Gabriella Carini; detector elements
- Relies heavily on Instrumentation Division
  - Under the leadership of Veljko Radeka it has a long history of developing detector elements for ionizing radiation (historically for HEP) and readout electronics
  - Has good technical resources (total staff ~45) including semiconductor foundry for detector elements, ASIC design, detector-readout bonding, custom PCB fabrication, standard board assembly and testing etc.
    - Pavel Rehak, Zheng Li, Wei Chen, Rolf Beuttenmuller; detector elements
    - Paul O'Connor, Angelo Dragone (SLAC), Gianluigi De Geronimo; ASIC design

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LDAC

- LCLS Detector Advisory Committee:
  - Gareth Derbyshire (chair): Rutherford Appleton Laboratory, UK
  - Erik Heijne (interim chair): CERN, Switzerland
  - Eric Eikenberry: PSI, Switzerland
  - Heinz Graafsma: DESY / XFEL, Germany
  - Ronnie Shepherd: LLNL, USA
  - Lothar Struder: MPI / Semiconductor Laboratory, Germany
  - Albert Walenta: University of Siegen, Germany
  - Yoshiyuki Amemiya: University of Tokyo, Japan
- Track technical progress, check if detector specs meet the original requirements and involved in technology choices
- Other topics e.g. DAQ and system integration
- LDAC report

Specifications

- Intense (10^{12} ph) and short (100 fs) pulses at 120 Hz need integrating detectors with fast readout (< 8 ms)
- Commercial detectors not available

	CXI	XPP	XCS
Readout noise	< 0.3 ph	<1 ph	<<1 ph
Full well capacity	1-10^3 ph	1-10^4 ph	1-100 ph
Pixel size	110 µm	90 µm	≤ 50 µm
Number of pixels	760^2 (1500^2)	1024^2 .	1024^2 .

- XPP: Multi-purpose detector to image the scattering intensity that is slowly varying with scattering angle (in steps) or a number of Bragg peaks on a low intensity background.
- XCS: Image the temporal changes in a speckle patterns that are related to the sample's dynamics; the pixel size should be ≤ speckle size.

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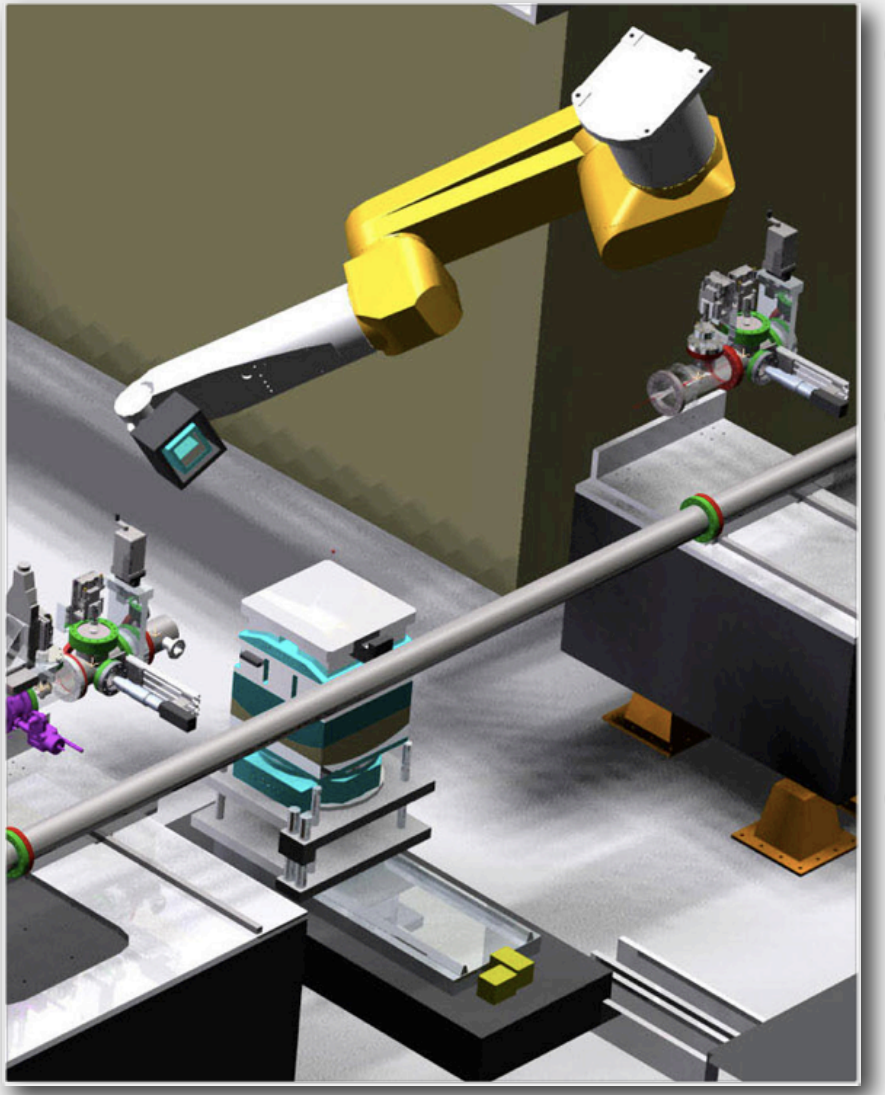
XPP Detector



- Diffractometer & robot arm
  - Sample - detector distance 10 - 100 cm
  - Quadrant of sphere
- Detector development:
  - Pixel sensor
  - Readout ASIC
  - DAQ
- Integration into XPP
  - Packaging
  - Mechanical interface
  - LCLS DAQ interface

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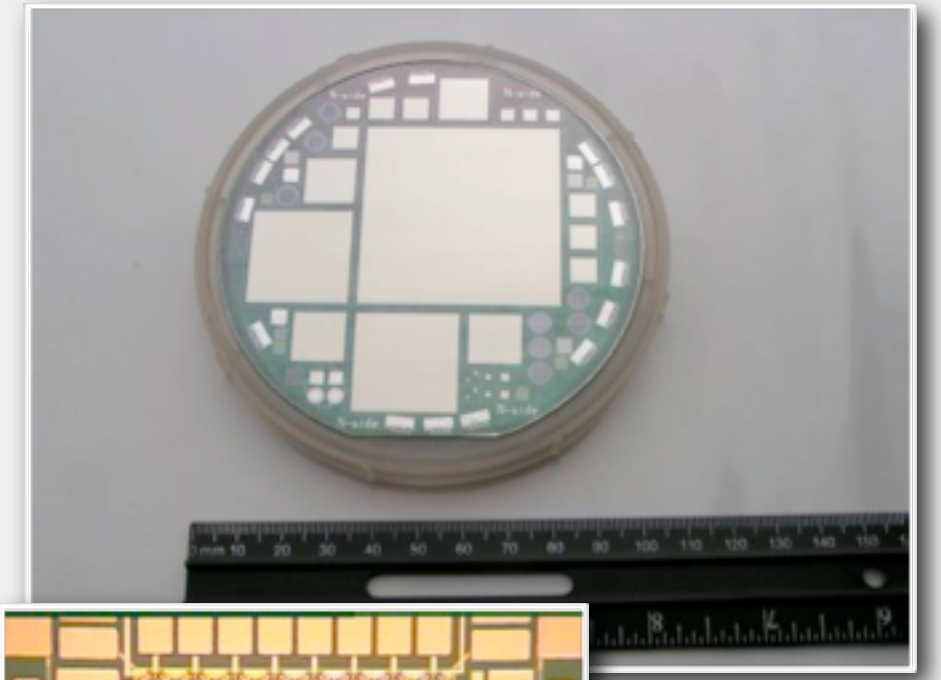
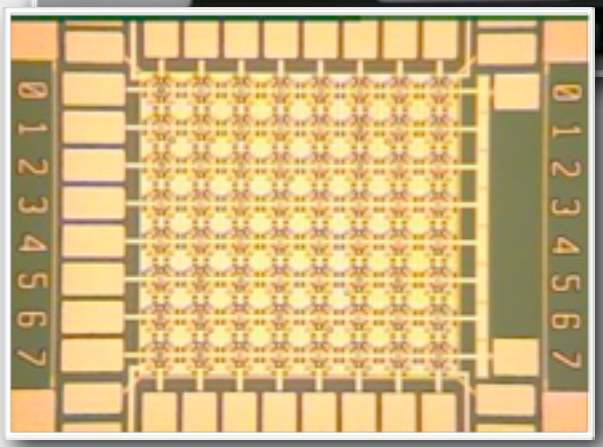
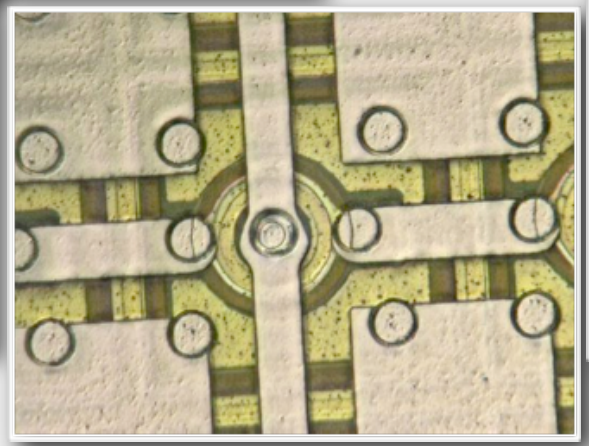
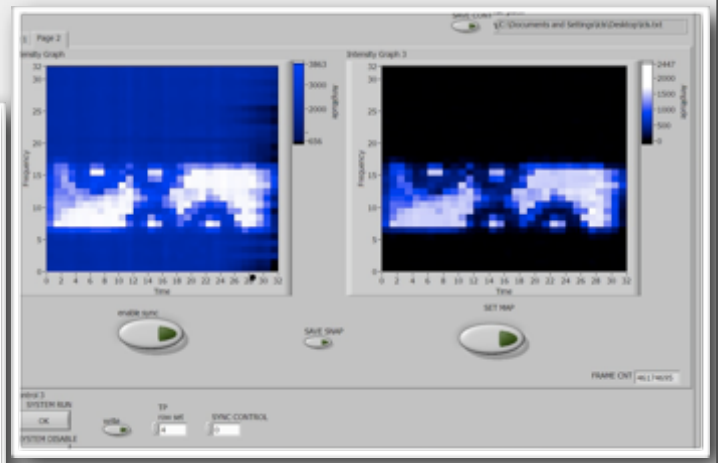
BNL XAMPS



- 512 x 512 module
  - 100 mm n-type wafer
  - 400 μm thick
- BNL in-house process
  - Critical: Vias and inter-metal layers
  - Transition from 100 to 150 mm
- X-rays with 32 x 32 module
- Assemble 64 x 64 module







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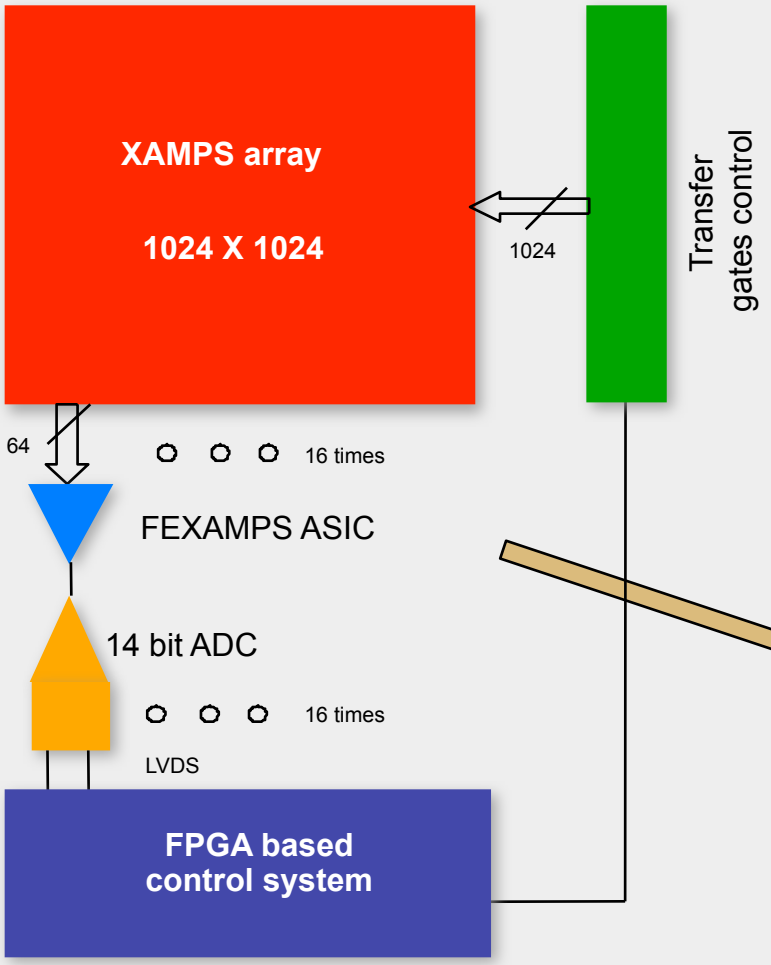
XAMPS Readout



- Switch-matrix structure; during data accumulation each row of pixels is switched on and the pixel charge is readout
  - Extremely challenging spec: >10^4 S/N, single-shot, fast readout

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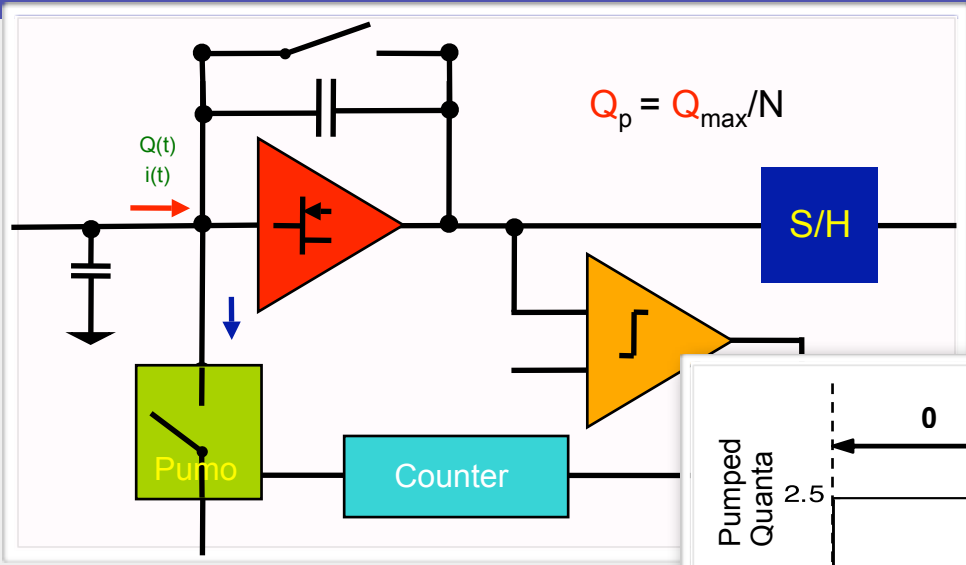
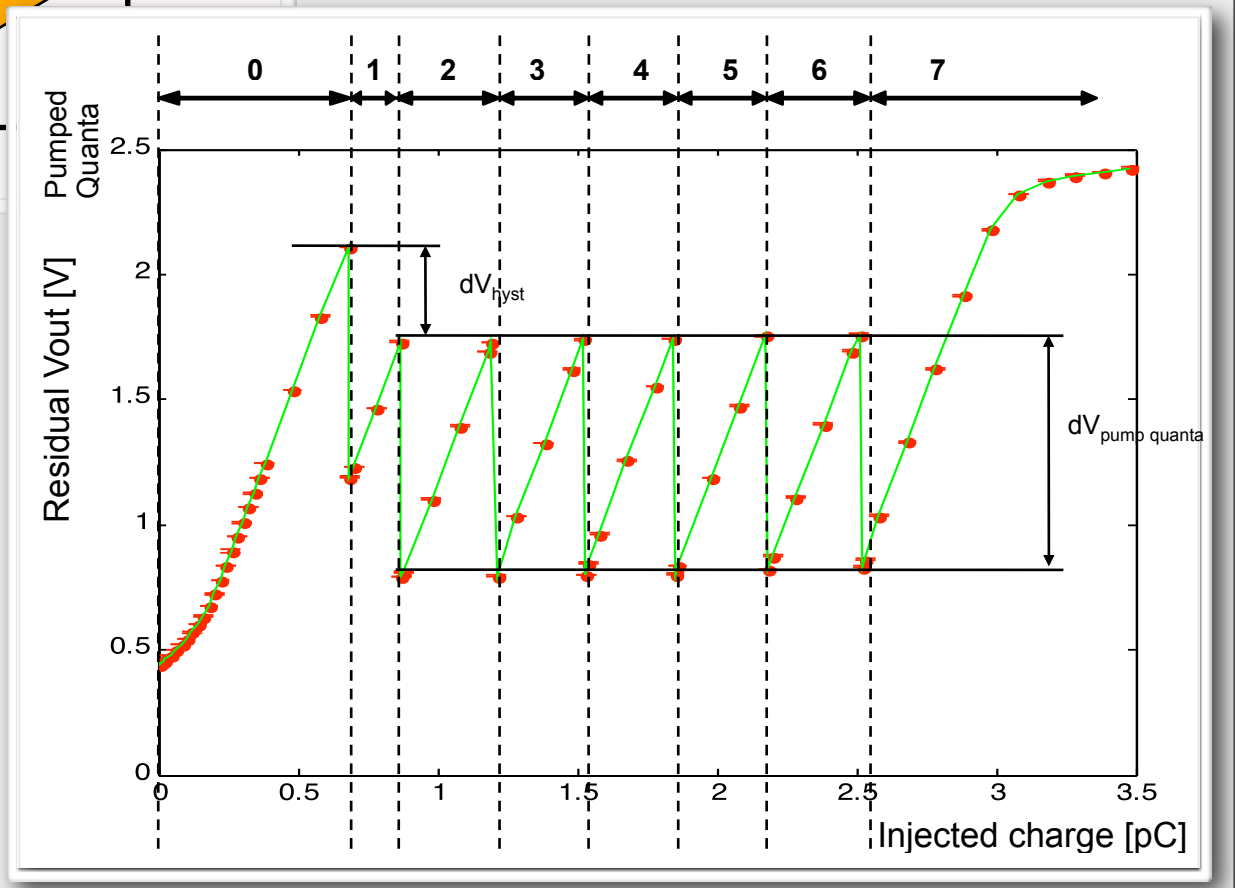
Readout ASIC



- Divide dynamic range into 8 intervals
- If $Q_{in} > Q_p$ remove (pump) a fixed amount of charge Q_p until the residual $Q_f < Q_p$
- Count number of removed quanta (3 bits)
- Sample the residual charge in C_f
- The output is converted with a 14 bit ADC (total 17 bit)



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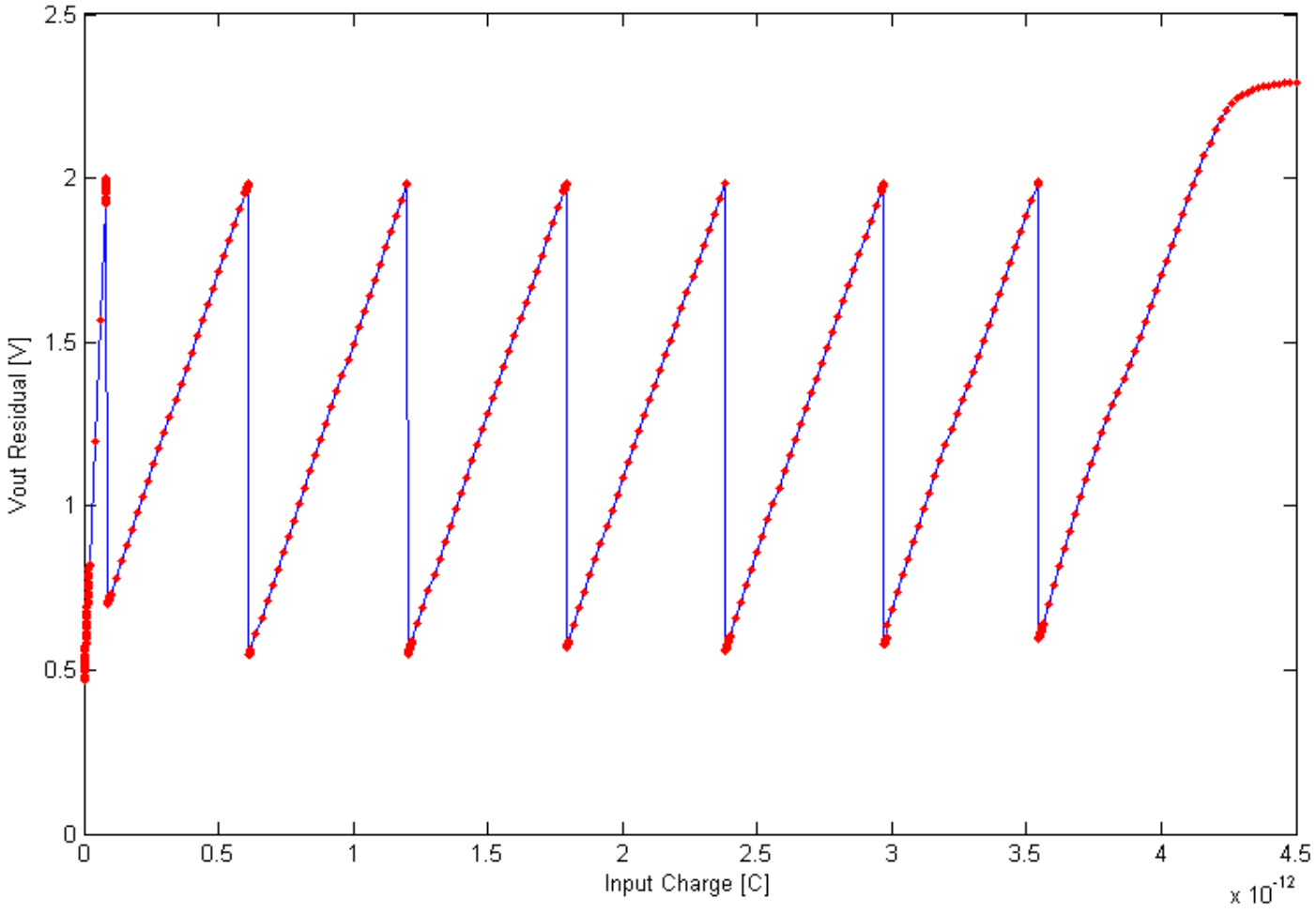
FEXAMPS 2



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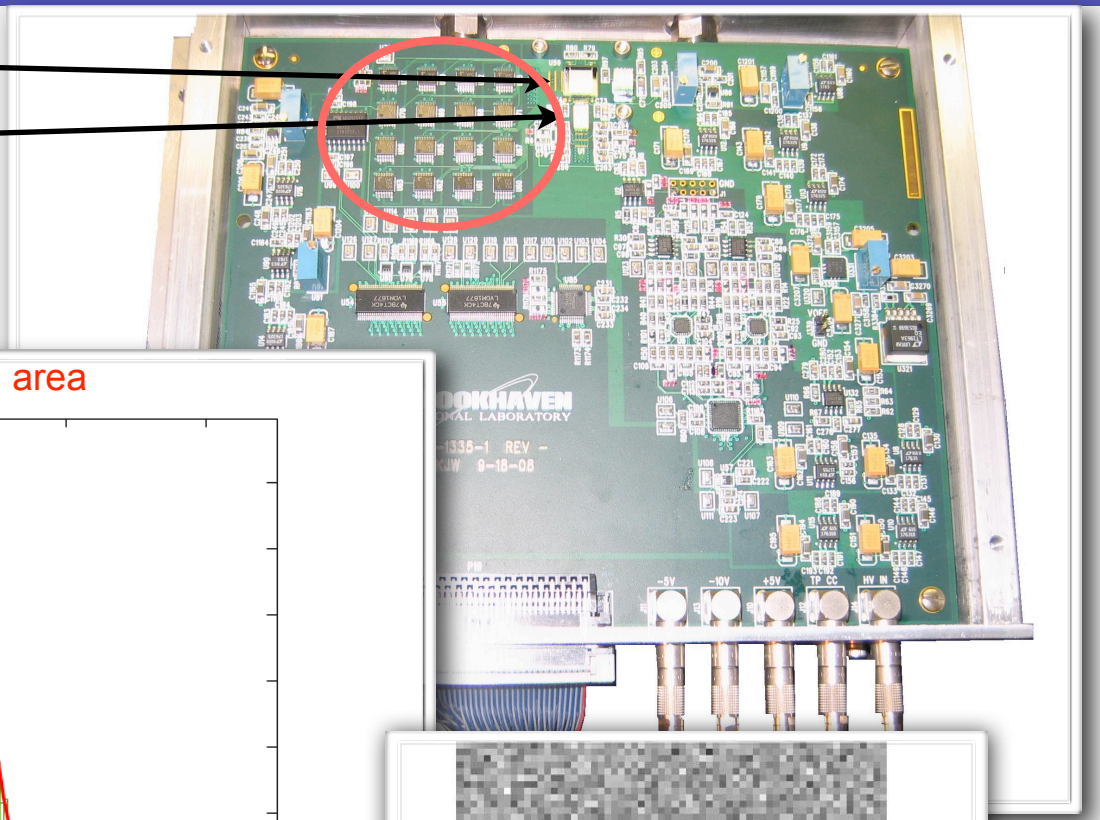
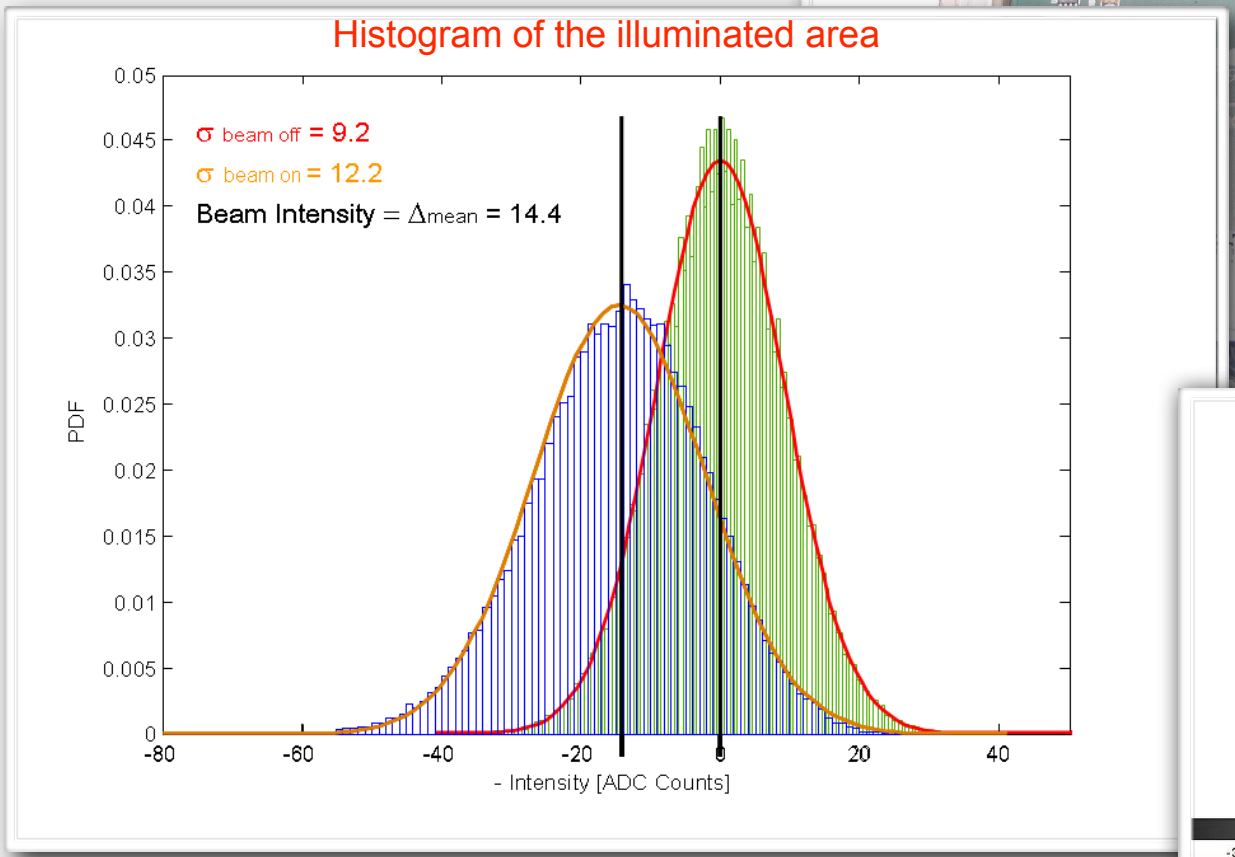
Detector tests with X-rays

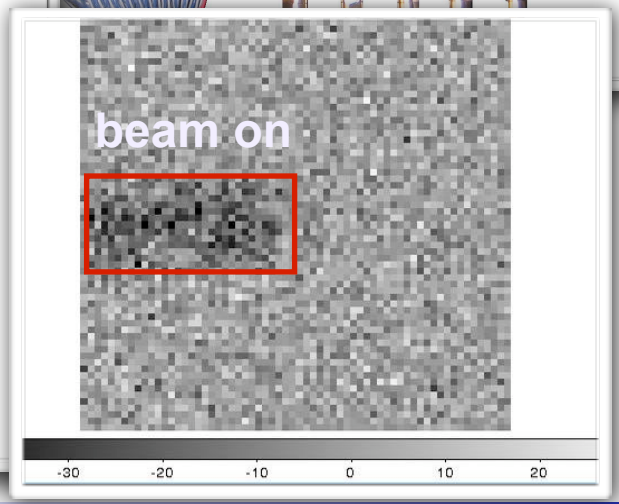
64x64 XAMPS Detector

FEXAMPS ASIC

Discrete Row Drivers







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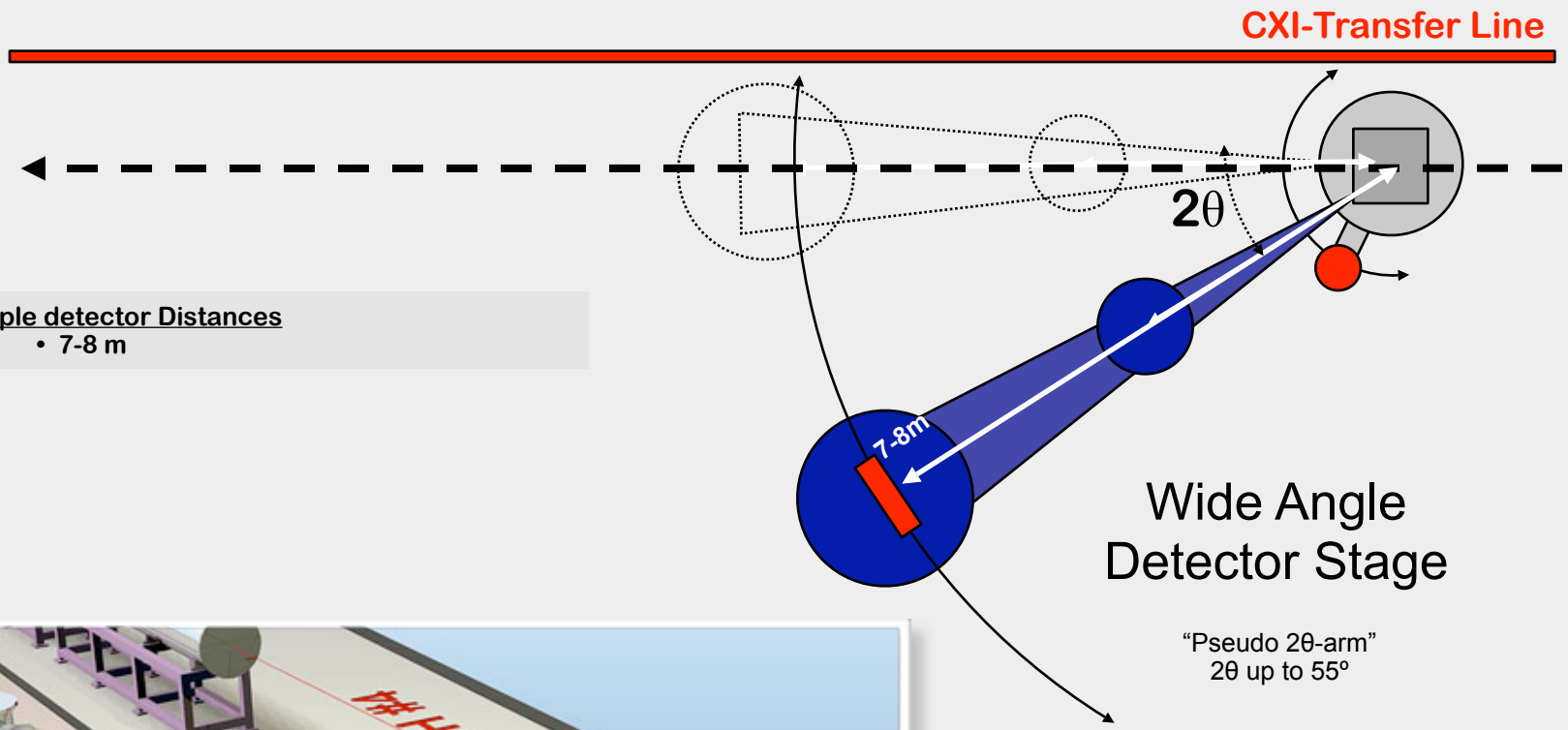
XCS Detector Stage

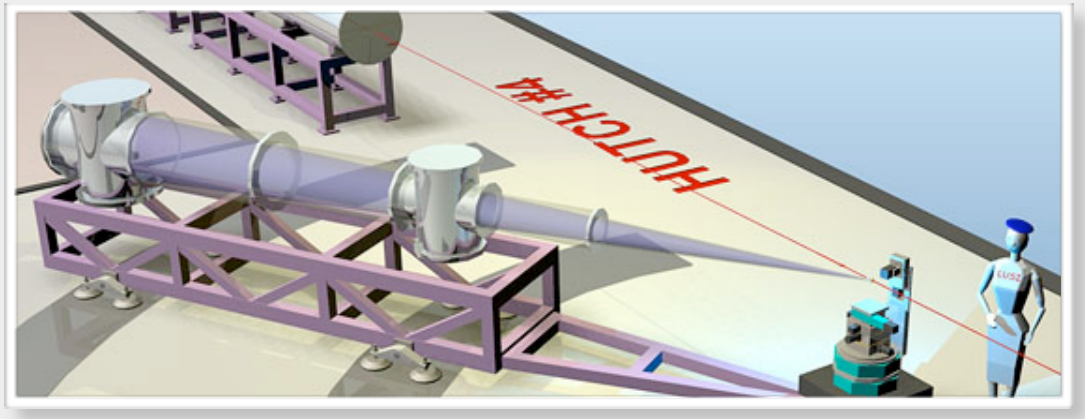


Sample detector Distances

- 7-8 m

Wide Angle Detector Stage

"Pseudo 2θ-arm"
2θ up to 55º



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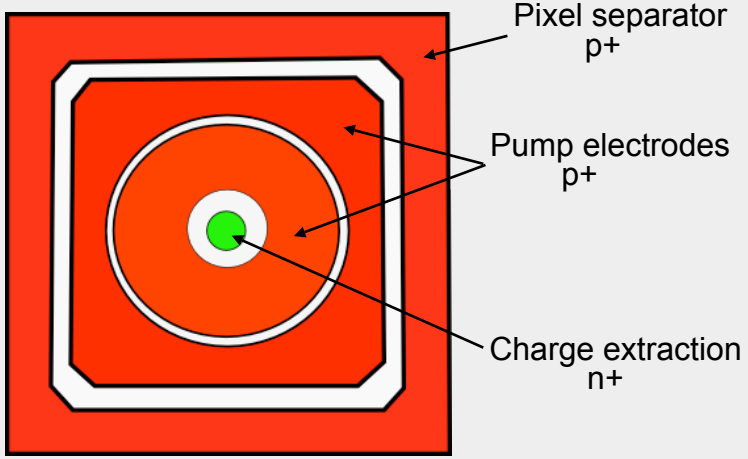
XCS Pixel



- "Charge-pump" structure for XCS experiments

  Charge is stored in a potential well and released in a controlled way similar to a drift detector

  - << 1 photon readout noise, needs different technology without transistor switch
  - Means that small pixels are possible (less DR).
  - No "kTC noise"

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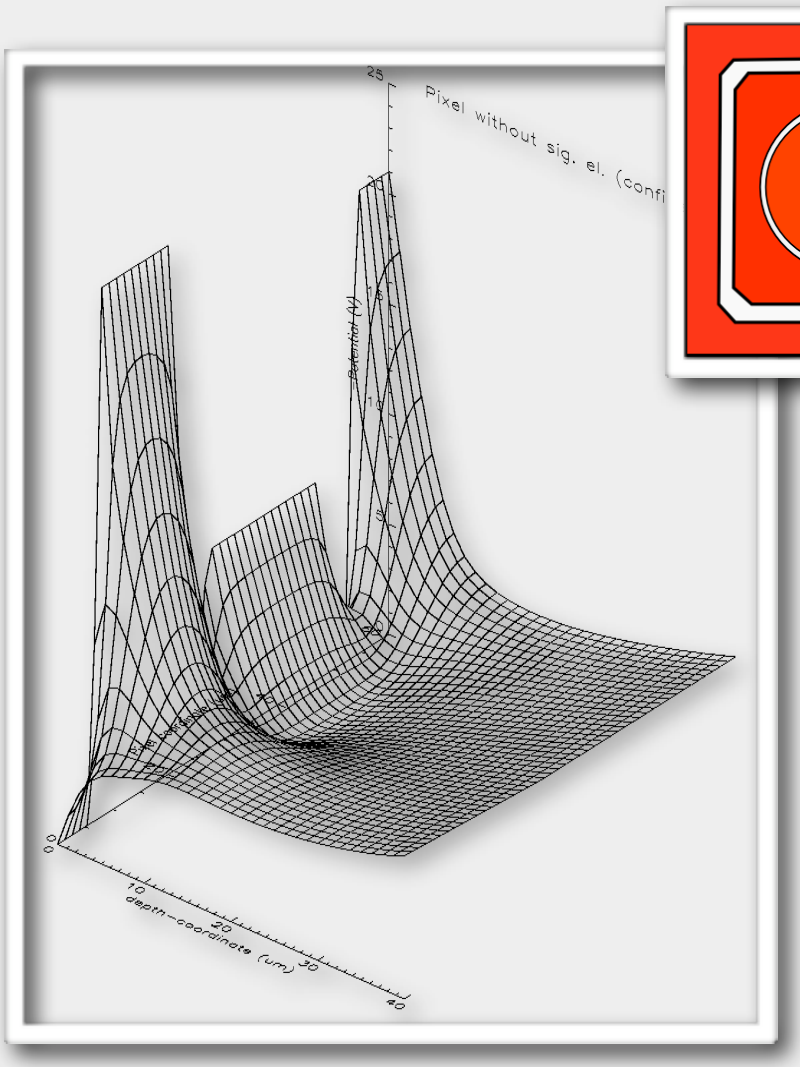
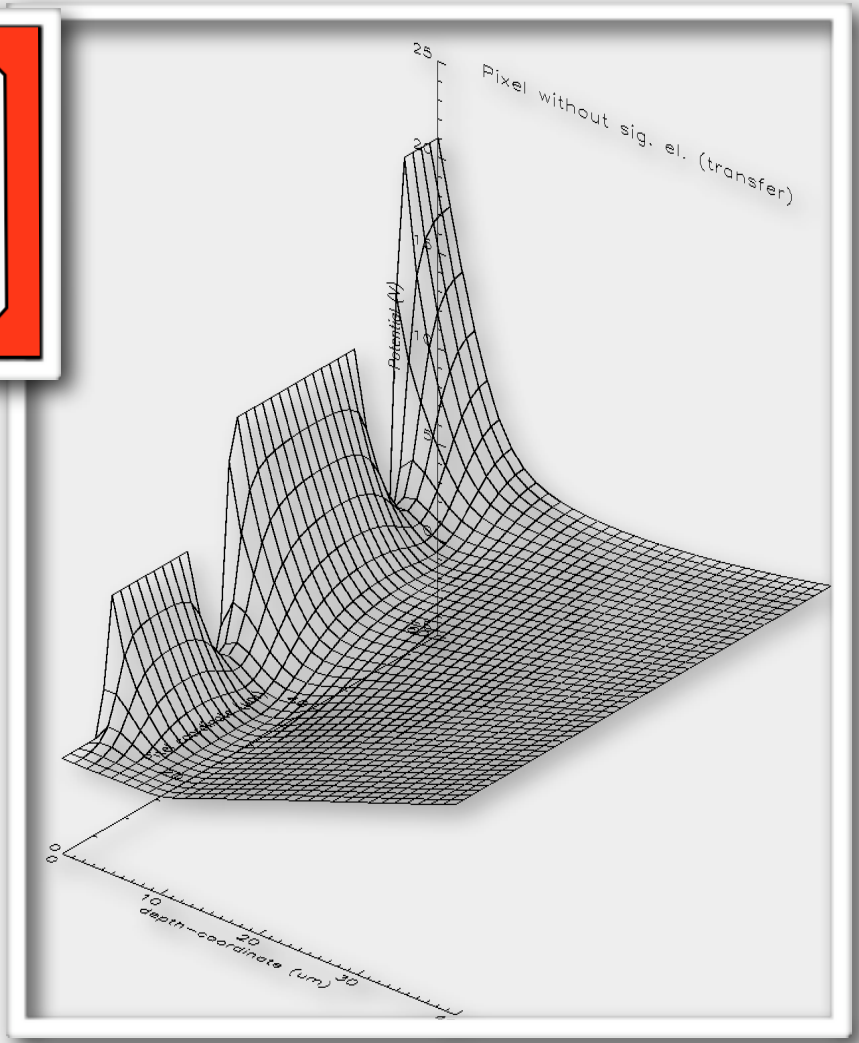
XCS Charge Pumping





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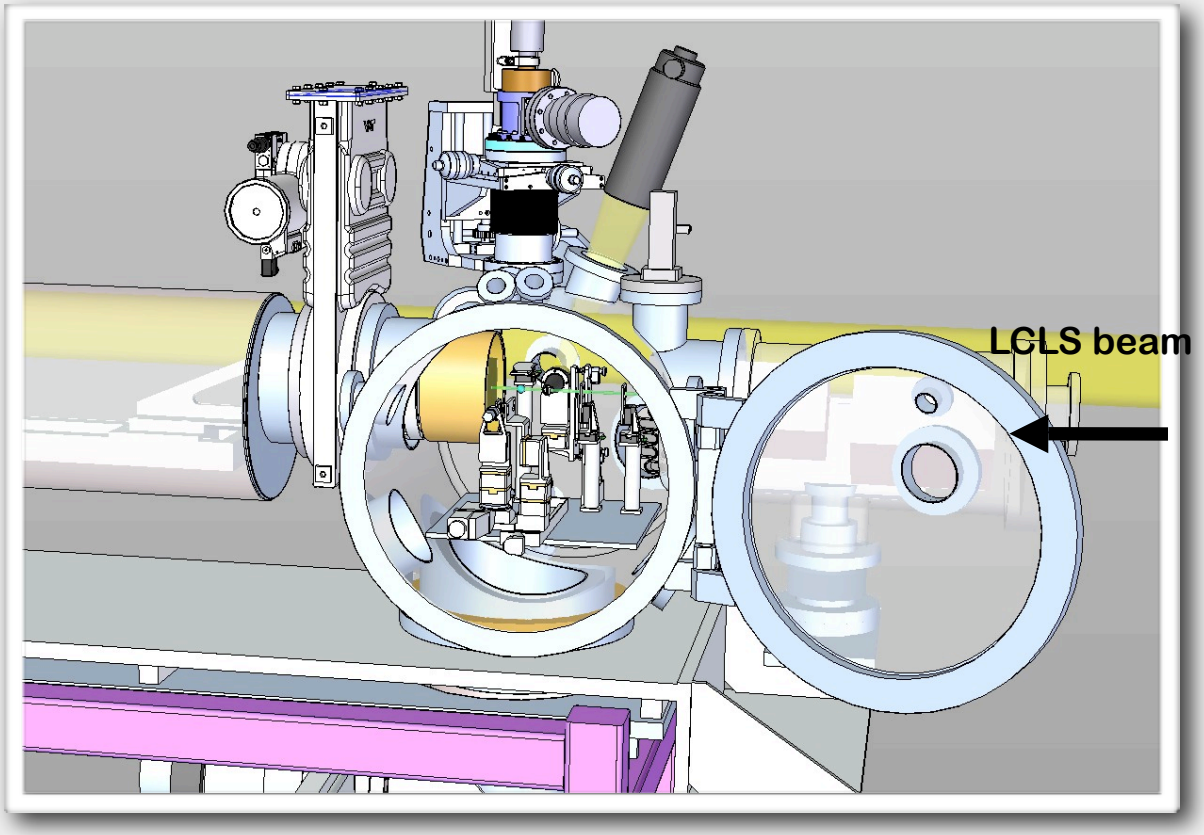
LDAC Recommendations

- Increase interaction with user community
  - Close interaction with Instrument Scientists
  - Team leader meetings & Instrument workshops
- BNL progress
  - Focus on evaluation of the in hand 512 x 512 sensor with x-rays
    - Try to reduce the sensor capacitance for better noise performance for single photons
    - Keep the 1024 x 1024 design in parallel: current boards & interfaces compatible with 1024
  - Need accurate planning with the deliveries of all system components
  - Find solution for clocking the detector rows: MPI ASIC
  - December 09: ‘compliments for the testing and evaluation of the readout chip, and for the first X-ray measurements with a 64x64 sensor”
- Adapt schedules to LUSI Instruments
  - Tight schedule to deliver the XPP detector in February 2010

CXI Detector



- Detector in vacuum 10^{-7} Torr
- Resolution depends on the sample-detector distance
  - Requires translation stage 700 mm
  - Remote Aperture resizing 1 - 10 mm
- Cooling 10 - 25 °C

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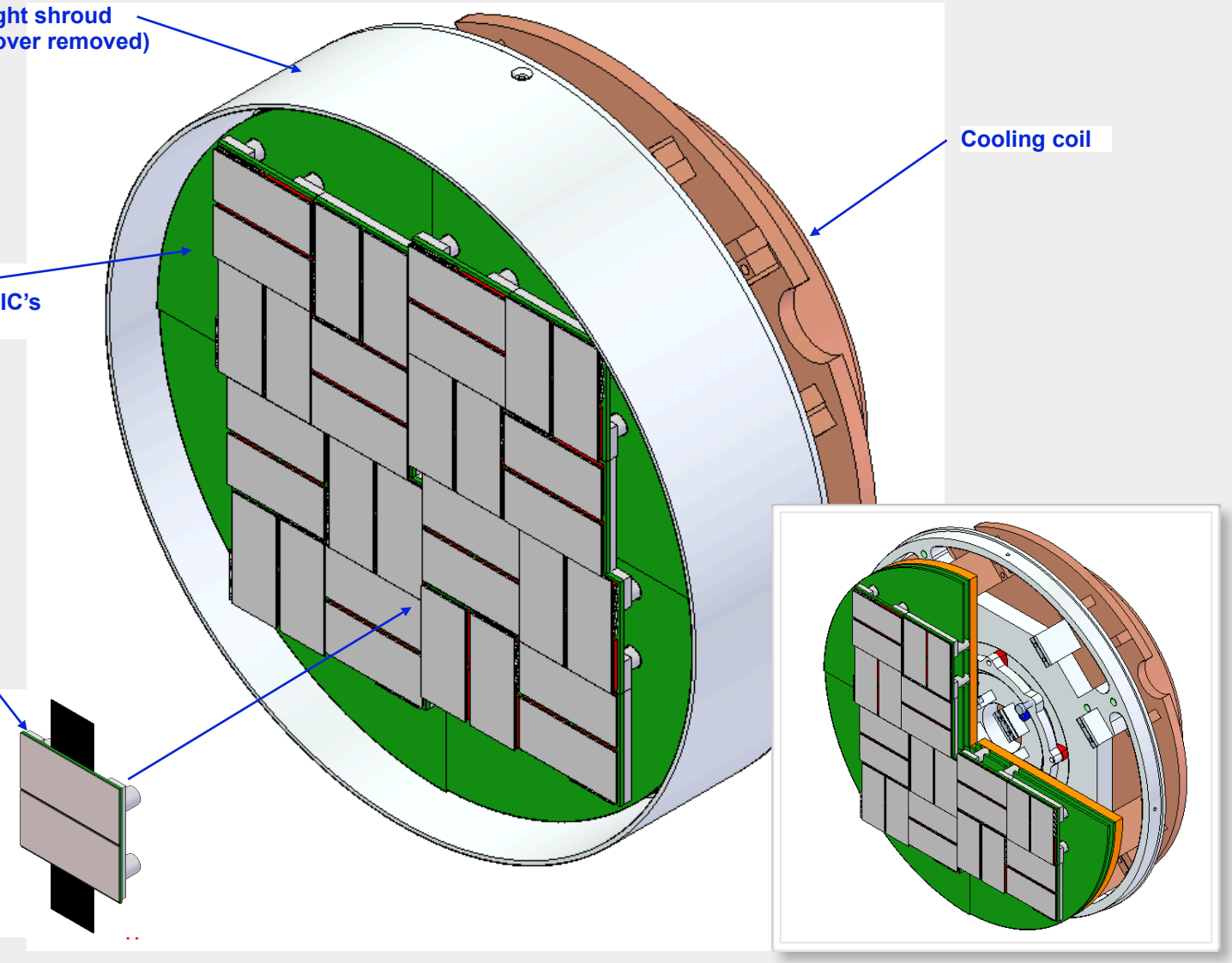
CXI Assembly



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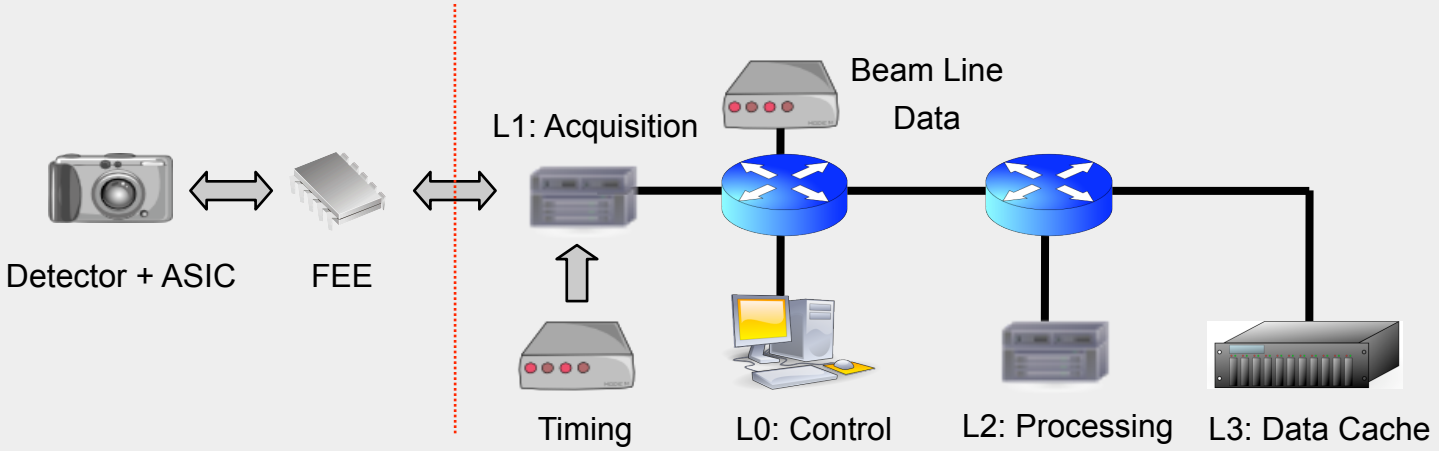
Detector - DAQ Interface



- Detector - Experiment Specific
- Front-End Electronics - Local configuration registers and state machines, FPGA used to transmit to DAQ system
- Timing info from the accelerator timing system, distributed to the detectors and L1 boards
- L0: DAQ operator consoles, control a run & configure the detector, telemetry monitoring
- L1: Acquire FEE data, detector calibration, event building, image processing, 10 Gb/s ethernet

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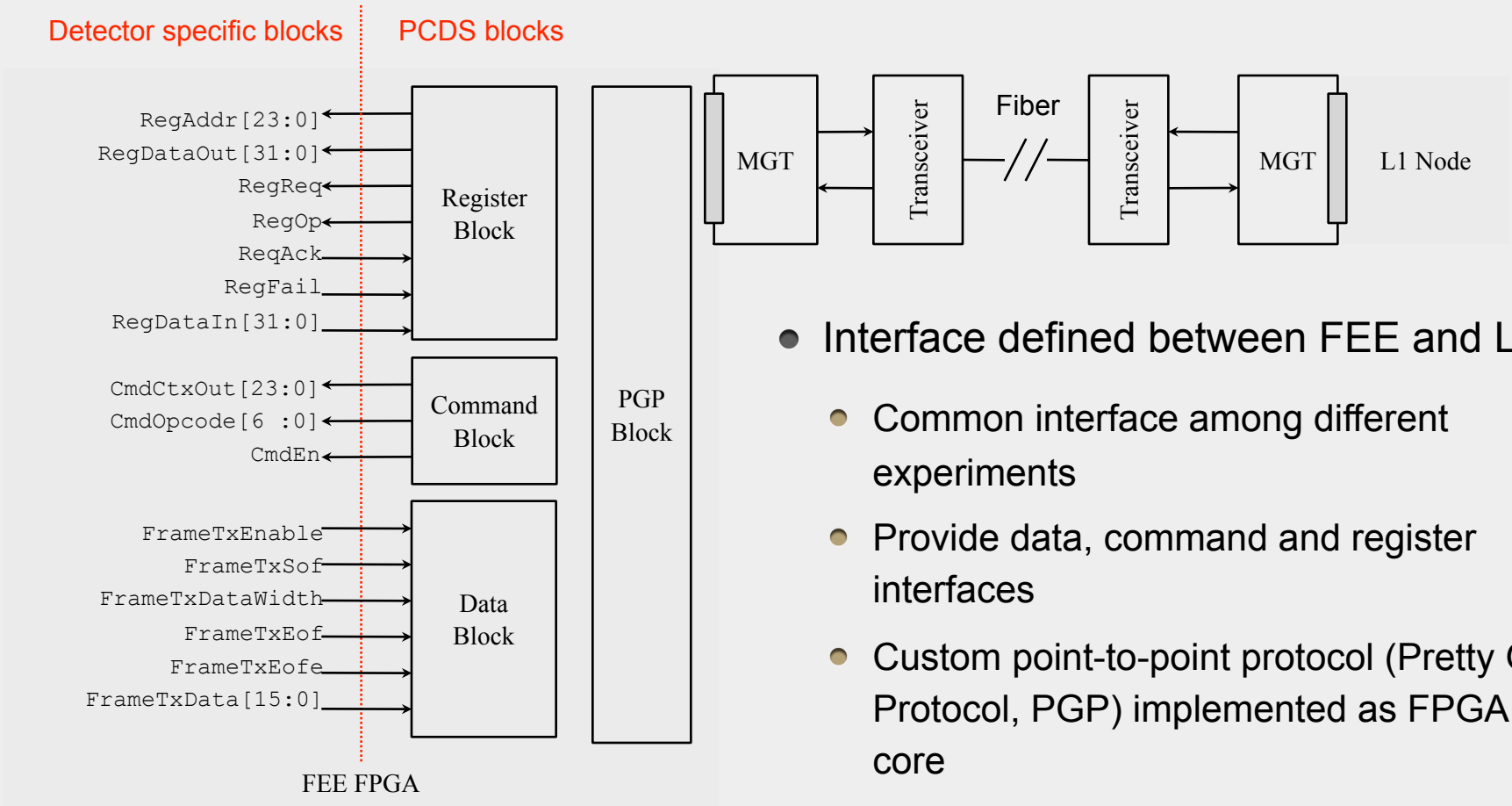
Register Command Data Interface



- Interface defined between FEE and L1
  - Common interface among different experiments
  - Provide data, command and register interfaces
  - Custom point-to-point protocol (Pretty Good Protocol, PGP) implemented as FPGA IP core
  - FEE FPGA assumed to be Xilinx family with Multi Gigabit Transceivers (MGT)

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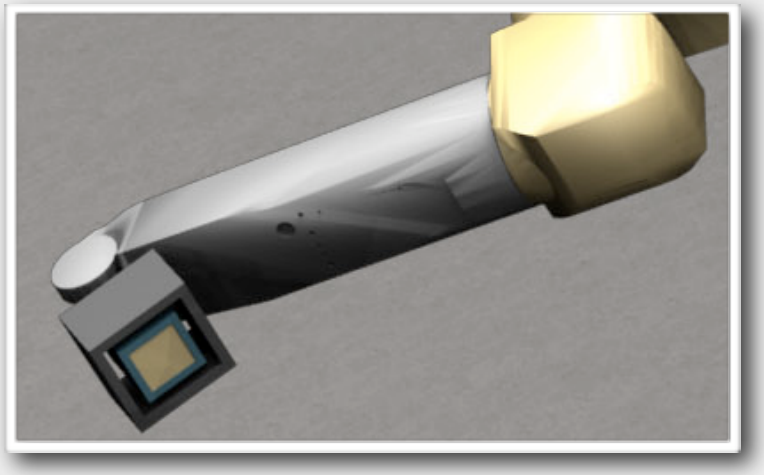
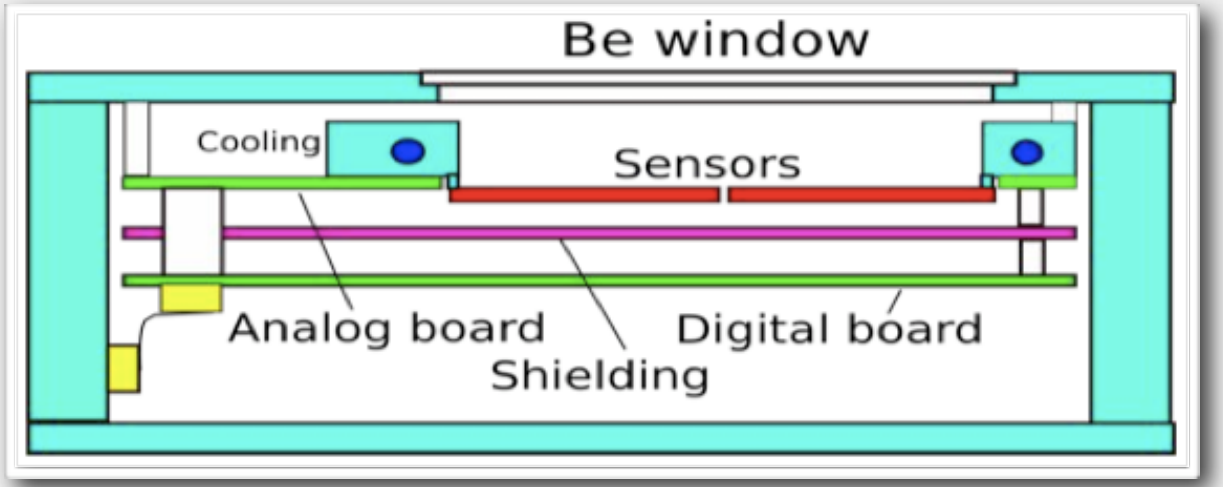
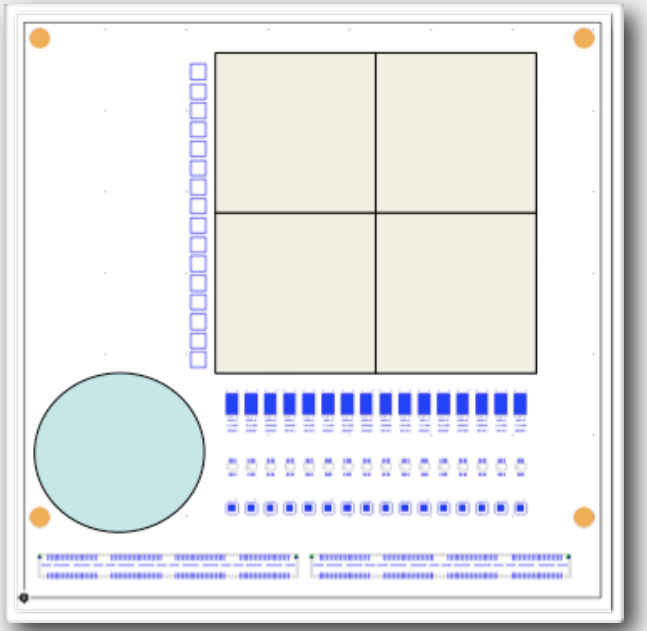
Mechanical Interface



- Aluminum base plate with
  - Robot mount
  - Alignment fiducials
- Detector Package
  - Analogue & Digital board
  - Cooling to stabilize T
  - Beryllium window

Update this slide





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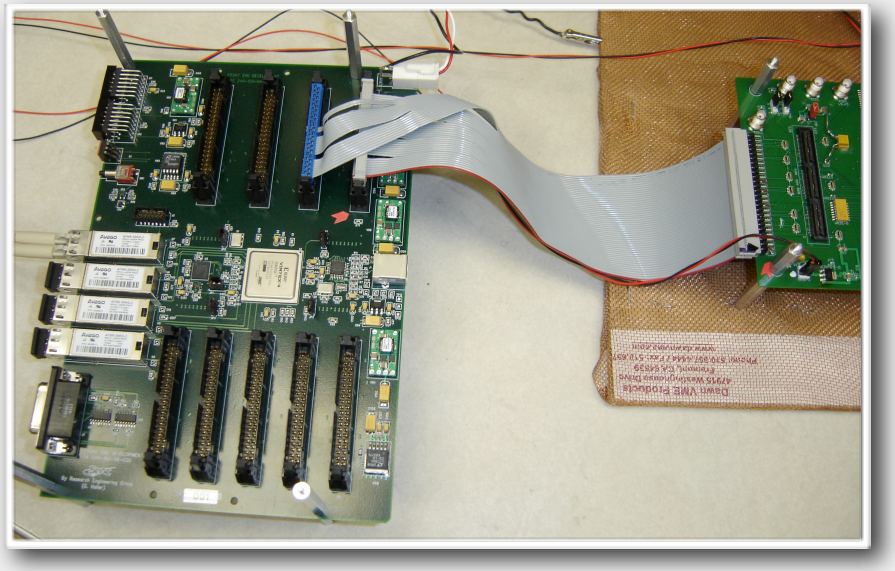
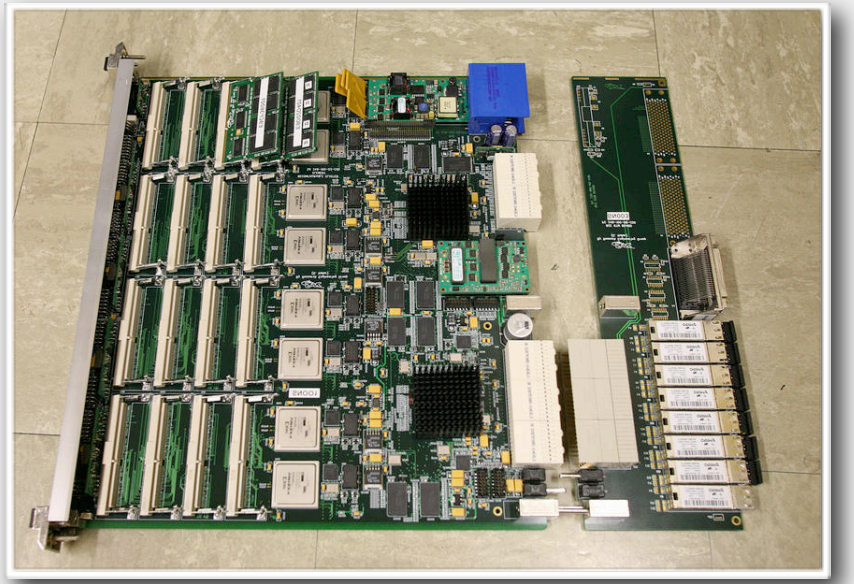
Detector Testing at SLAC



- SLAC Front End Development board
- Additional testing; feedback to Detector Groups
- Improves integration into LCLS & LUSI instruments

- SLAC custom made ATCA board
- Based on System On Chip (SOC) Technology: Xilinx Virtex 4 (6)
- System Memory Subsystem: 512 MB of RAM, 8 GB/s throughput
- Configuration Flash Memory Subsystem: 128 MB for storing software code and configuration parameters (up to 16 images)



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Summary

- Cornell 2D PAD detector at SLAC September 2009
  - CXI ready in April 2011
- BNL XAMPS detector at SLAC February 2010
  - XPP ready in July 2010
- BNL XCS detector at SLAC October 2011
  - XCS ready in June 2011
    - Duplicate XPP detector needed March 2011

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Acknowledgments

- LCLS & LUSI Scientists
- BNL: Peter Siddons, Pavel Rehak, Zheng Li, Wei Chen, Gabriella Carini, Paul O'Connor, Gianluigi De Geronimo, Angelo Dragone
- SLAC DAQ: Gunther Haller, Amedeo Perazzo, Mark Freytag, Mike Huffer, Chris O'Grady, Leonid Sapozhnikov, Eric Siskind, Dave Tarkington, Matt Weaver
- SLAC Mechanics: Martin Nordby, David Nelson, Matthew Swift, Don Schafer
- SLAC Testing: Ryan Herbst, Dieter Freytag
- Cornell: Sol Gruner, Hugh Philipp, Mark Tate, Marianne Hromalik, Lucas Koerner

Back-up

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