LCLS BPMs

Patrick Krejcik
Steve Smith
Ron Johnson
Evgeny Medvedko
Till Straumann

Overview

- Requirements
- BPM Types
  - Striplines
  - Cavities
- BPM Processor Concept
- Status
- Planned Work

LCLS BPMs

- Measurement of transverse position of electron beam trajectory
- ~150 BPMs along the machine (injector, linac, LTU, undulator, dump)
- Positional resolution requirement 1..20um @0.1nC (R~10mm)
- Two different physical devices
  - Striplines (5-10um resolution)
  - Cavities (< 1um resolution)
- Use existing linac striplines

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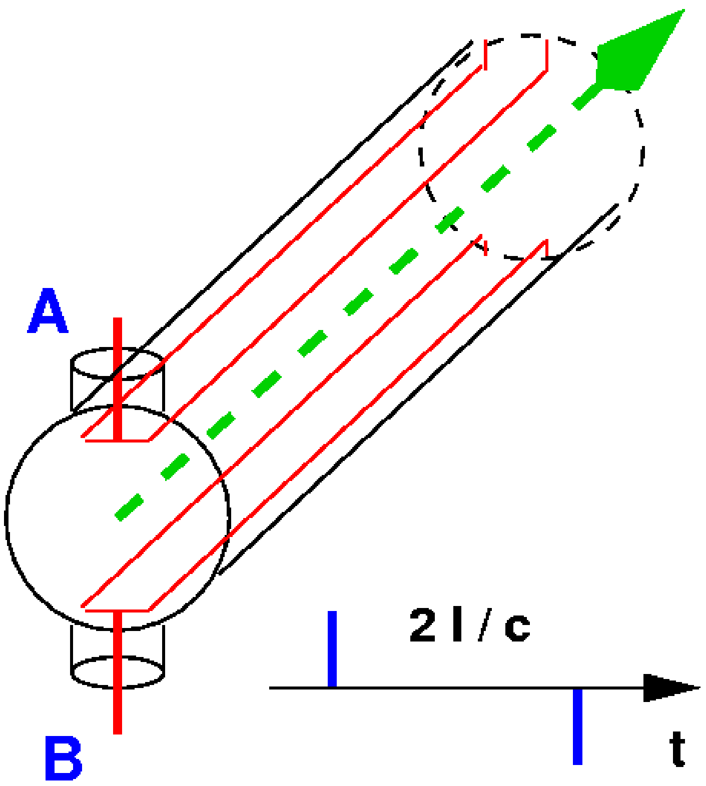
Lcls-controls@slac.stanford.edu

Stripline BPM

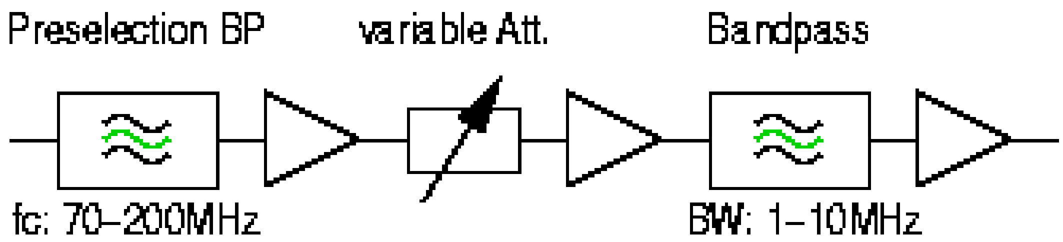
- Short electron bunch induces wideband pulse doublet
- Positional information is small difference of large numbers (~5E-3)
- Y/R~ 4 (A-B) Q



Stripline BPM Electronics

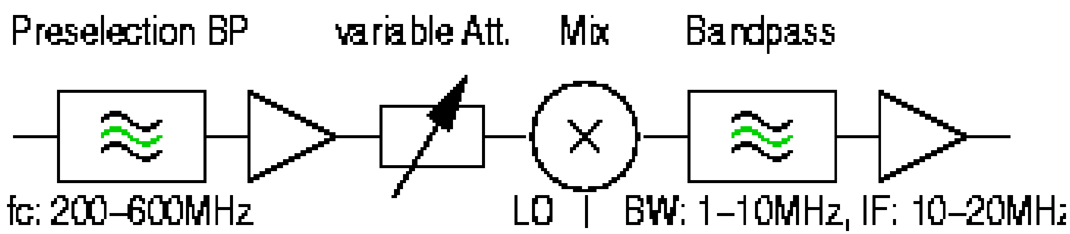
- Backend
  - Wideband ADC (state of the art: 14bit, 100MSPS, 200MHz input signal BW)
- Frontend
  - Limit bandwidth (“ring a filter”)
  - Set processing center frequency (undersample, mixer)
  - Match signal level to ADC
  - Optional: difference “A-B” in hybrid
- Normalize to bunch charge (e.g., (A-B)/(A+B))
- Calibration (offset, gain)

Analog Frontend Electronics (Stripl)



No conversion of processing freq.

- Simple; more sensitive to ADC and clock

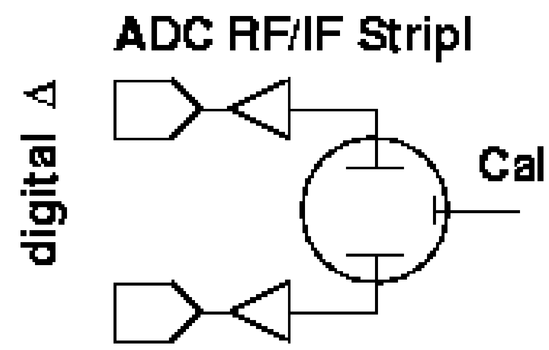


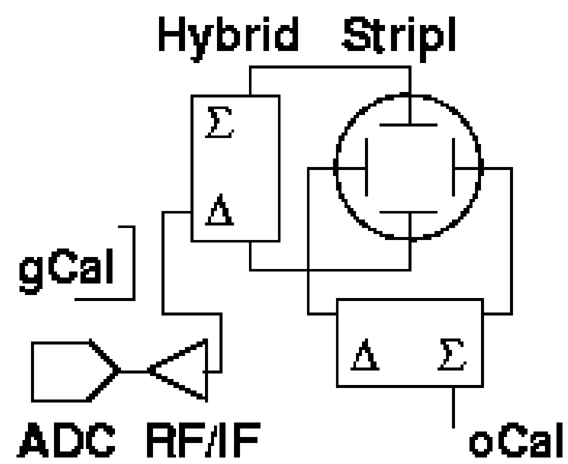
Heterodyne receiver

- Higher freq. Possible; needs LO

Frontend Processor Options

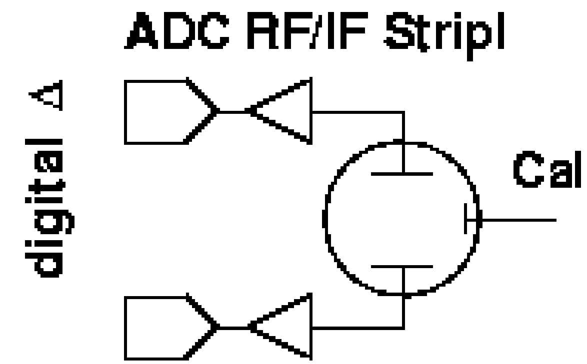
- Digital Difference
  - Easy gain/offset calibration
  - Requires higher dynamic range
  - More channels needed
- Analog Difference
  - Less channels
  - Bunch charge info needed
  - Reduced dynamic range
  - Relies on hybrid symmetry (?)

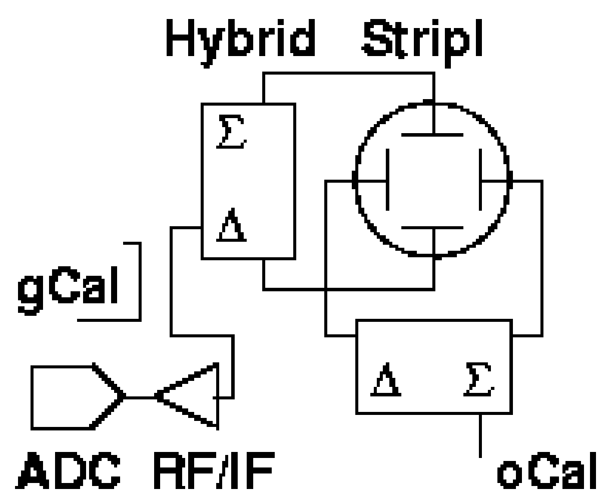




Calibration

- Inject calibration signal to orthogonal strips
  - Takes care of gain and offset
  - Sensitive to imbalance of active parts (diff. of big numbers)
- Inject to sum port of orthogonal hybrid
  - Relies only on symmetry of strips
  - Less sensitive (drift of active parts)
  - Separate gain cal. Needed



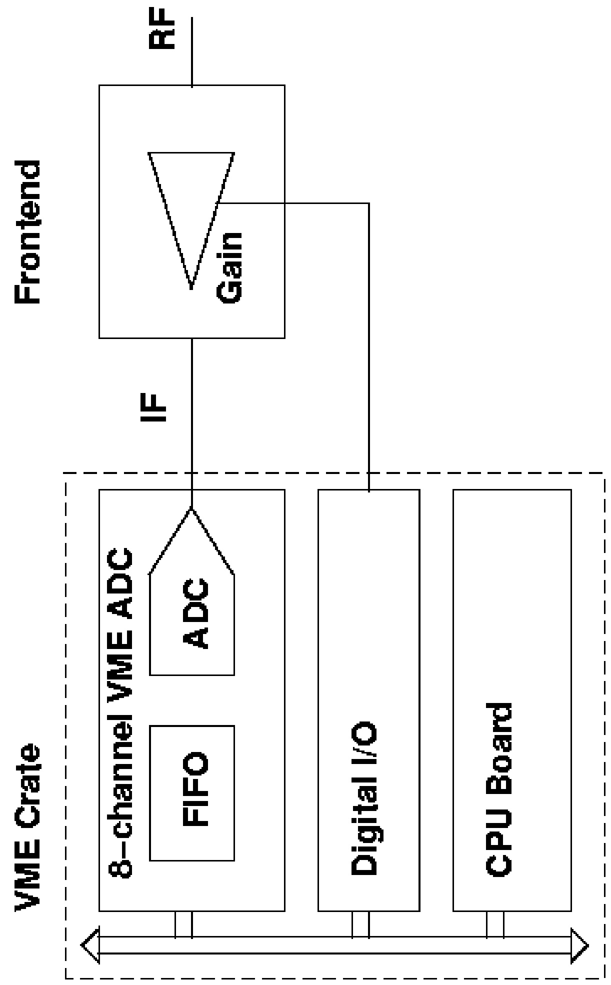


Important Design Parameters

- Processing frequency (cable losses, stripline response)
- Processing bandwidth (tradeoff analog SNR vs. processing gain to reduce digitizer noise)
- Linearity (if calculating difference in digital domain)
- Noise Figure (low bunch charge)

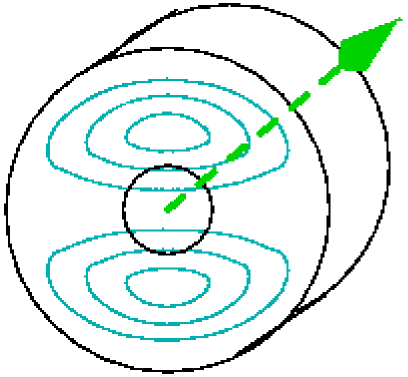
BPM Processor -- Controls

- Commercial VME digitizer (8 channels/card)
- Slow backplane
- Digital I/O for gain control; calibration
- Ext. trigger
- “Scalar processor”
- Optional: digital receiver to reduce backplane & processing load



Cavity BPMs

- Excitation of dipole mode by off-center beam
- Sensitive to position and angle
- No response at center
- Reference cavity needed
  - Phase info ("up" vs. "down")
  - Normalize to bunch charge
- Problem: suppression of monopole mode
- C- or X- band operation
- Complex Calibration (mechanical?)



Cavity BPM Processor

- Use same backend as for striplines (VME digitizer)
- “Vector processor” because phase info needed
- 2-stage heterodyne frontend
- Is a mechanical positioning subsystem necessary? (work at ATF: 3 BPMs in a sophisticated mechanical positioning setup).

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Status

- Understand critical design parameters and processing algorithms
- Conceptual design
- Identified VME digitizers. Evaluation modules ordered
- Prototype for a 140MHz (wrong freq.) analog front-end is being built (Smith)
- Looked at Libera solution. Doesn't seem to be useful for our application.

Next Months

- Evaluation of Echotek VME digitizer
- Prototype front-end for stripline BPMs
- Run tests on live beam
- Test “Hybrid solution”
- Test calibration schemes, stability