

# Detectors for Diffraction Measurements at the LCLS

## 1) Summary

The LCLS repetition rate of 120 Hz requires the development of high frame rate area detectors for x-ray diffraction measurements. Such detectors will be needed in experiments involving single molecule x-ray diffraction, high energy density physics and femtochemistry as well as potentially other areas. The requirements in general are similar to those for synchrotron-based diffraction experiments, ie. high efficiency, single photon detection sensitivity, a large number of pixels and a large dynamic range, but with the central additional feature that the frame to frame time must be commensurate with the repetition rate of the LCLS. Due to the large amount of data that will be produced, in many cases some form of real time data compression must also be used. We therefore need to go from the 1 Hz frame rates of present day detectors for diffraction experiments to 120 Hz frame rates for the LCLS, while maintaining or in some cases extending the performance in terms of noise and dynamic range. This represents a major challenge for detector development and for LCLS experiments.

The detector of choice for synchrotron diffraction experiments at present is the phosphor screen-based, fiber coupled CCD (Gruner, Tate et al., 2002) . This type of detector is commercially available, and it typically has all the required attributes listed above, except that normal frame to frame time are 1 second or longer. The strategy proposed here therefore is to take this standard and robust detector technology and simply speed it up and add external processing power, to make it compatible with the requirements of the LCLS. In order to provide the frame to frame speed required, we propose to make a column parallel form of CCD, utilizing a multi-channel readout CMOS microelectronic chip. Instead of reading by clocking out line by line and then for each line serially shifting data out through one output node, data is clocked out in parallel through an array of identical readout channels connected to each column, or to a small set of columns via a shift register. The frame to frame time is speeded up by number of parallel channels employed.

LBNL is uniquely set up to provide this type of technology to LCLS experiments. LBNL's strength in this area is our ability to leverage our experience as the premier US pixel detector laboratory, via our development of the readout electronics for the ATLAS pixel detector, along with our unique CCD experience, based on the development of thick, fully depleted CCDs for SNAP. In addition, we have a full program to develop wide dynamic range radiation-hard readout for these CCDs including a novel multi-slope CDS and pipelined ADC along with an integrated CCD controller. The high-speed readout proposed here will be implemented in custom integrated circuits, which will use demonstrated SNAP concepts as a starting point, adapted to the needs of LCLS.

The Supernova Acceleration Probe (SNAP) is a satellite-based telescope that uses a focal plane detector array of 36 CCDs (Rhodes, Refregier et al., 2004) . The CCDs are back illuminated fully depleted devices for high quantum efficiency and extended performance in the near IR region (Bebek, 2003) (see also [www.snap.lbl.gov](http://www.snap.lbl.gov)). Due to the high number of CCDs being used as well as space considerations, the readout electronics are monolithic microelectronic CMOS devices; these include multi-slope charge integrators, correlated double sampling and pipelined ADC electronics. The intent here then is to utilize the existing experience at LBNL in the SNAP project, and to build a massively parallel CCD. Again, utilizing our experience in high energy physics detectors such as ATLAS, given the large data volume,

we will implement feature extraction and data compression algorithms in FPGAs or DSPs directly coupled to the pipelined ADCs. As part of the development, we will optimize those data compression functions which can be performed directly on-chip, and those which are best performed immediately off-chip.

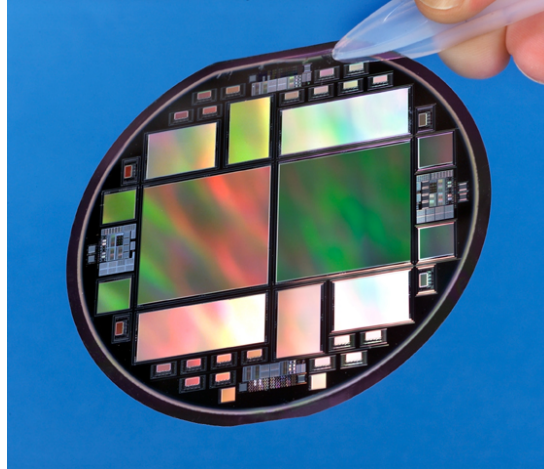
The project we propose here consists of two parts, firstly an R&D phase in which a complete single CCD element and back end will be constructed and tested and a second phase in which a complete detector system will be constructed and tested. The latter will consist of a pair of detectors separated along the beam direction, with each being arranged as a 2 x 2 array to allow a small aperture to be located at the center. The first will operate as a wide angle x-ray detector and the second as a small angle x-ray detector. Use of two detectors in series with appropriate sensitivities will allow a very large dynamic range to be measured. In other cases where a more modest dynamic range is required, a single module could be used. In other cases a single quadrant could be used. In order to provide an estimate of costs, we have assumed that a single quadrant will be produced and tested, followed by two 2x2 modules with all associated processing electronics.

We intend to work with Fairchild Imaging (Milpitas, CA) from the outset so that their expertise in production of specialized CCDs and camera systems can be brought to bear on this project, and so that there is an assured route to commercialization built into the project. Fairchild are the only US manufacturer that combines both in-house CCD manufacture as well as production of complete CCD-based x-ray area detectors and are therefore a logical choice for this collaboration. We have had extensive initial discussions with Fairchild management regarding this collaboration and are agreed on the outline for this work.

In order to kickstart this development process, a grant for funding development of column parallel CCDs for x-ray detection has just been obtained under the LBNL Laboratory Directed Research and Development (LDRD) program. This has been funded at ~ \$460k in FY05, ie. from October 2004.

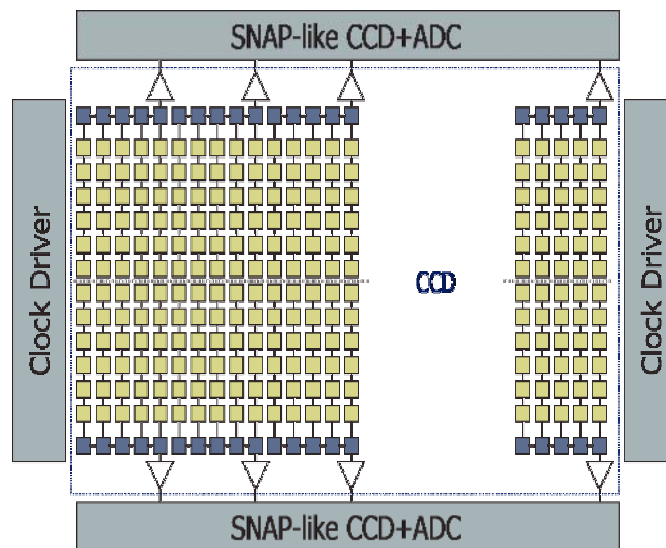
## 2) A SNAP-based column parallel readout CCD.

CCDs are arrays of MOS capacitors. Polysilicon gate lines run horizontally over the surface of the CCD, and channel stop diffusions run vertically. In a conventional 3-phase CCD, a pixel is defined by the area between two channel stops covered by three polysilicon lines. To readout the CCD, data are shifted vertically into another CCD structure that acts as a horizontal shift register. The horizontal shift register is then clocked out to an ADC. Just before the ADC, the CCD charge is converted to a voltage (via a floating diffusion node with small capacitance). As the signal is typically then driven off-chip, a buffer amplifier is needed to drive the load capacitance. If there are  $v$  pixels in a column, and  $h$  pixels in the horizontal shift register, then the horizontal clock frequency must be  $f_h = h f_v$ , where  $f_v$  is the vertical clock frequency, and the frame rate is  $f = f_v/v$ . Note that the frame rate is independent of the length of the horizontal shift register, but not the horizontal clock frequency, which is  $f_h = h v f$ .



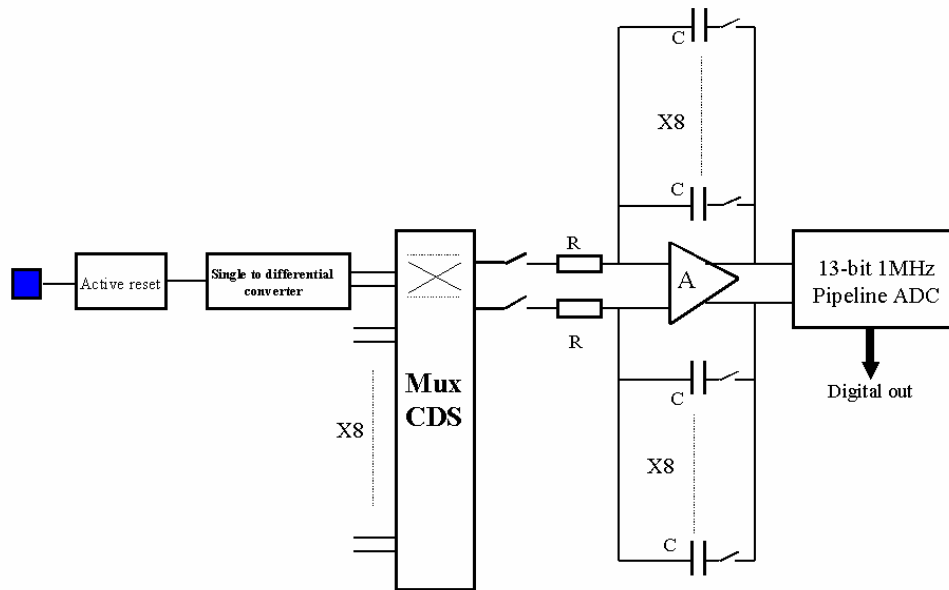
**Fig. 1** CCDs designed and fabricated at LBNL for the SNAP project

In order to increase the frame rate, conventional high-speed CCDs have 4-port readout. Dividing the CCD in half vertically, and adding a second horizontal shift register on top, gives an immediate factor of two speed increase in the frame rate for a given vertical clock frequency. Splitting the CCD horizontally reduces the speed requirement for the ADC by an additional factor of two. Further increases of the frame rate require further subdivision. Adding more vertical subdivisions is difficult, so the only way to increase the frame rate is to increase the vertical clock frequency. The vertical clock frequency cannot be arbitrarily high, as the clocking speed is limited by the intrinsic RC time constant of the gate lines. For high-quality imaging, back-illuminated CCDs are assumed, which allows the use of metal strapping – running metal lines in parallel above the polysilicon lines and contacting the two. To go beyond this, we must go to the column parallel readout architecture, where data is vertically clocked either to individual readout nodes associated with each column, or where columns are grouped with short serial shift registers for horizontal clocking.



**Fig. 2** Column parallel architecture with short horizontal shift registers

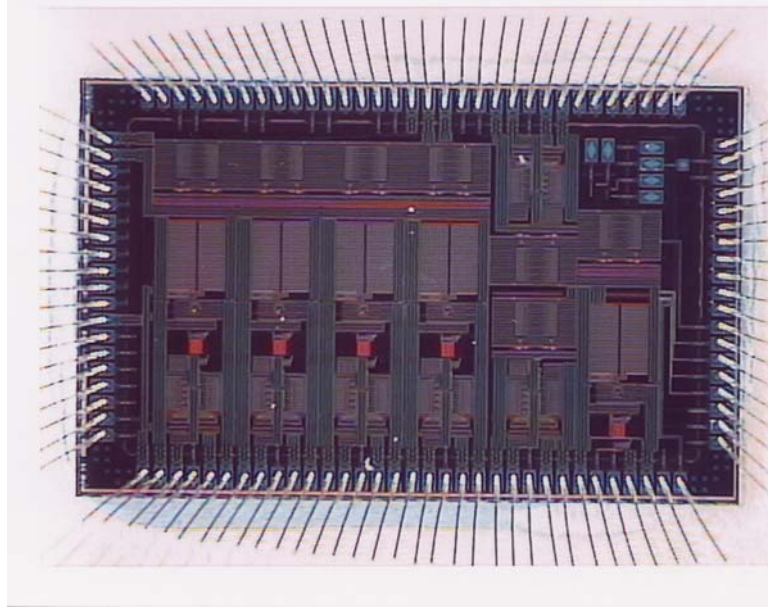
The major development item for a high-speed CCD is the associated readout electronics. Given the high circuit density, integrated circuits are required. In order to reduce the cost, LBNL is considering two approaches, both based on the floating point integrator/correlated double sampler and pipelined ADC developed for SNAP. The first approach would be to have a large number of readout ports with short serial shift registers. For an initial target of 1k x 1k, and 5 ms readout time, the vertical frame rate would be 100 kHz . 10-pixel horizontal shift registers then give a horizontal (ADC) frequency of 1 MHz, as well as a layout pitch of 300 (400)  $\mu\text{m}$  using 30(40)  $\mu\text{m}$  pixels) . The CCD and readout circuits would be placed on a hybrid, and wire bonds would connect the two. The second approach would be a fully column-parallel readout, in which every column has a port. In this case, a 1k x 1k 40  $\mu\text{m}$  pixel front-illuminated CCD would be bump-bonded to readout chips.



**Fig. 3** Block diagram of the CRIC (Ccd Readout Integrated Circuit) chip for SNAP consisting of a multiplexed correlated double sampler and multi-slope integrator with pipelined ADC

In either case, the most appropriate readout technique uses a differential averager which consists of a correlated double sampler (CDS) followed by an integrator. The integrated circuit will consist of 128 CCD readout channels. Each channel consists of a source follower, an active reset module and a single to differential converter. Eight of these channels are multiplexed in to CDS and a switch capacitor array multi-slope integrator followed by a 13 bits pipeline ADC; note that the effect of the multislope integrator is to give a dynamic range of > 16 bits (Walder, Chao et al., 2003) . The 16 ADC's are read out in parallel. Figure 3 shows the block diagram for 8 channels.

When CCD's are read out they generate two output levels for each pixel sample. The first value is the reset value of the cell. The second value is the video level. During readout of the CCD each channels reset level and video level would be integrated onto one set of capacitors in the feedback of the integrator. Dependent on the charge in the pixel the capacitor value would be chosen, in real time, to match the signal level.



**Fig. 4.** CRIC CCD readout chip fro SNAP

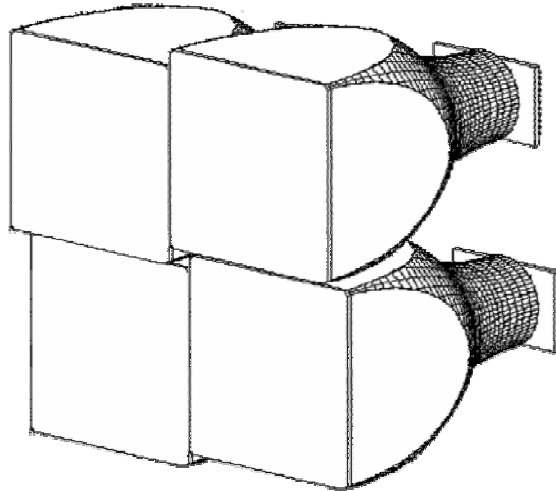
For both types of CCD, a fiber-optic would be used to connect the CCD to the phosphor. In the column-parallel design, there is no source follower at the end of each column, as the low capacitance of the bump bond obviates the need. Each column would have a correlated double sampler, and the outputs can then be multiplexed N::1 into an ADC. The SNAP integrator and ADC would also be used, with either the SNAP CDS, or the Fairchild “Active Reset” CDS.

### **3) Specific program for LCLS applications**

As can be seen from section 2 above, we plan to reuse much of the very substantial design and investment made in SNAP. This allows us to rapidly move to a robust solution for LCLS in a cost effective and predictable manner.

The architecture described above will have a  $< 5$  msec frame to frame time for  $1k \times 1k$ , 16 bits dynamic range and single photon sensitivity. Developing this single module will be the 1<sup>st</sup> task of the project and will take approximately 2 years, following our initial 1 year of LDRD funded design work.

The second phase of the project will be to design, construct and test one complete  $2 \times 2$  module. The individual CCDs will be slightly offset to produce a small hole in the center, allowing light to pass on to either a second complete  $2 \times 2$  module further downstream or a backstop or beam monitor. This arrangement is shown in Fig. 5. The taper is shown exaggerated. In reality, the taper angle will be close to zero. The taper is only required so that there is space for electronics and wiring connections.



**Fig. 5** 2 x 2 array of basic fiber coupled CCD elements; these are shown offset to allow x-rays to pass through the center and with a much larger taper angle than will be used in practice.

The idea of using small angle and a wide angle detectors in series allows one to adjust the sensitivity of the second detector so that a wider dynamic range can be achieved than with a single detector. However, in some cases it is quite likely that the 16 bit dynamic range of one detector array module will be sufficient. It seems therefore advantageous that the detectors should be as short along the beam direction as possible, and stackable. We also need to examine whether we can use one detector, with a much smaller central hole, and with an attenuator in the small angle region, almost in contact with the phosphor screen; this again would have the effect of extending the dynamic range; the attenuation would be measured and then removed in analysis. The ideal arrangement would be to have a thin optical attenuator between the output of the fiber optic and the CCD in the small angle region; this would eliminate the possibility of scattering in the previous arrangement. These ideas can be easily tested on normal SAXS systems, such as BL 12.3 (Sibyls) at ALS.

The 1<sup>st</sup> CCD (2k x 2k, 30 micron pixels, therefore 60 mm on edge) would be between 30 and 60 mm from the sample typically; the hole size in the 2x2 array would be around 10 mm. The second detector would have to have a much smaller hole. In principle the detectors could be identical, but a very important point is that we want to minimize distance to the sample (and hence pixel size) in order to minimize parasitic scattering from the residual background. To overlap the SAXS and WAXS regions, would imply that the detectors would have to be an enormous distance apart, and so in the 2 detector situation, for reasons of reducing scattering in the 2<sup>nd</sup> detector to a minimum, we will have to have a very small hole, something of the order of 0.5 mm or less. The practical layout will be experiment dependent and needs to be studied in detail. Due to the extreme data rates, as high a degree of data compression will be done on camera as possible. Due to the coherent nature of the source and non-crystalline nature of samples, simple compressions schemes cannot be used. However, it may well be possible for example to fit the overall 2d scattering shape with a simply described polynomial for background, and then export only the small deviations from this value; this would result in significant compression. These will be tested during year 1. The compression computations will be carried out in Field Programmable Gate Array (FPGA) chips in real time (ie. full frame computation and data extraction and storage commensurate with the 120 Hz LCLS repetition rate)

The tasks on a year by year basis will be:

**Year 1 (LBNL LDRD funded in FY05)**

This year will be funded by LBNL LDRD and will concentrate on adaptation of SNAP electronics to the needs of LCLS and initial design and testing of a few complete electronics channels.

- a) IC design (modification of CRIC chip)
- b) IC test (on few channels)
- c) IC characterization
- d) simulation of data and compression schemes
- e) evaluation of experimental design parameters such as camera and pixel size, attenuation masks etc.

Cost: personnel 0.35 M\$ (with lower LDRD overhead)

**Year 2 (1<sup>st</sup> year of LCLS project)**

- a) fabrication of full 1k x 1k readout
- b) test of full readout chip
- c) mechanical design
- d) FPGA design and simulation
- e) design of back end computing system
- f) CCD design and fabrication

Cost : personnel 1.3 M\$, hardware 0.3 M\$

**Year 3 (2<sup>nd</sup> year of LCLS project)**

- a) assembly of CCD to 1k x 1k readout system
- b) testing of complete module
- c) fabrication of backend electronics and FPGA
- d) testing of system at high data rates in simulated LCLS data conditions
- e) fabricate and start tests on complete 2 x 2 module

Cost: personnel 1.4 M\$, hardware 0.3 M\$

**Year 4 (3<sup>rd</sup> year, to be completed 6 months into FY)**

- a) complete tests on 1<sup>st</sup> 2 x 2 module
- b) assemble and test 2<sup>nd</sup> 2 x 2 module
- c) complete back end computing systems
- d) documentation

Cost: personnel 0.4 M\$, hardware 0.2 M\$

**TOTAL:** personnel and equipment, including LBNL overheads **\$3.9M**

#### 4) Project team

P. Denes	PI and Project Leader
H. A. Padmore (& ALS ESG)	Co-PI and detector specification and testing
H. von der Lippe	Microelectronics Leader
J-P Walder	Microelectronic systems
J-M Bussat	Microelectronic systems
B. N. Krieger	Microelectronic systems
E. Mandelli	Microelectronic systems

#### 5) Contact information

Peter Denes  
Deputy Division Director for Electronics, Software and Instrumentation Engineering  
Lawrence Berkeley National Laboratory, MS 50A6134 ,  
1 Cyclotron Rd., Berkeley, CA94720  
Phone (510)486-6471 : e-mail (PDenes@lbl.gov)

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